Data General

Technical Manual

6052 -6053 DISPLAY TERMINAL

(Preliminary)

015-000065-00

NOTICE

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC's equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC, prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

DGC reserves the right to make changes without notice in the specifications and materials contained herein and shall not be responsible for any damages (including consequential) caused by reliance on the materials presented, including but not limited to typographical or arithmetic errors, company policy and pricing information. The information contained herein on DGC software is summary in nature. More detailed information on DGC software is available in current released publications.

NOVA, SUPERNOVA, ECLIPSE and **NOVADISC** are registered trademarks of Data General Corporation, Southboro, Mass.

Ordering No. 015-000065
© Data General Corporation, 1976
All Rights Reserved
Printed in the United States of America
Revision 00, November 1976

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

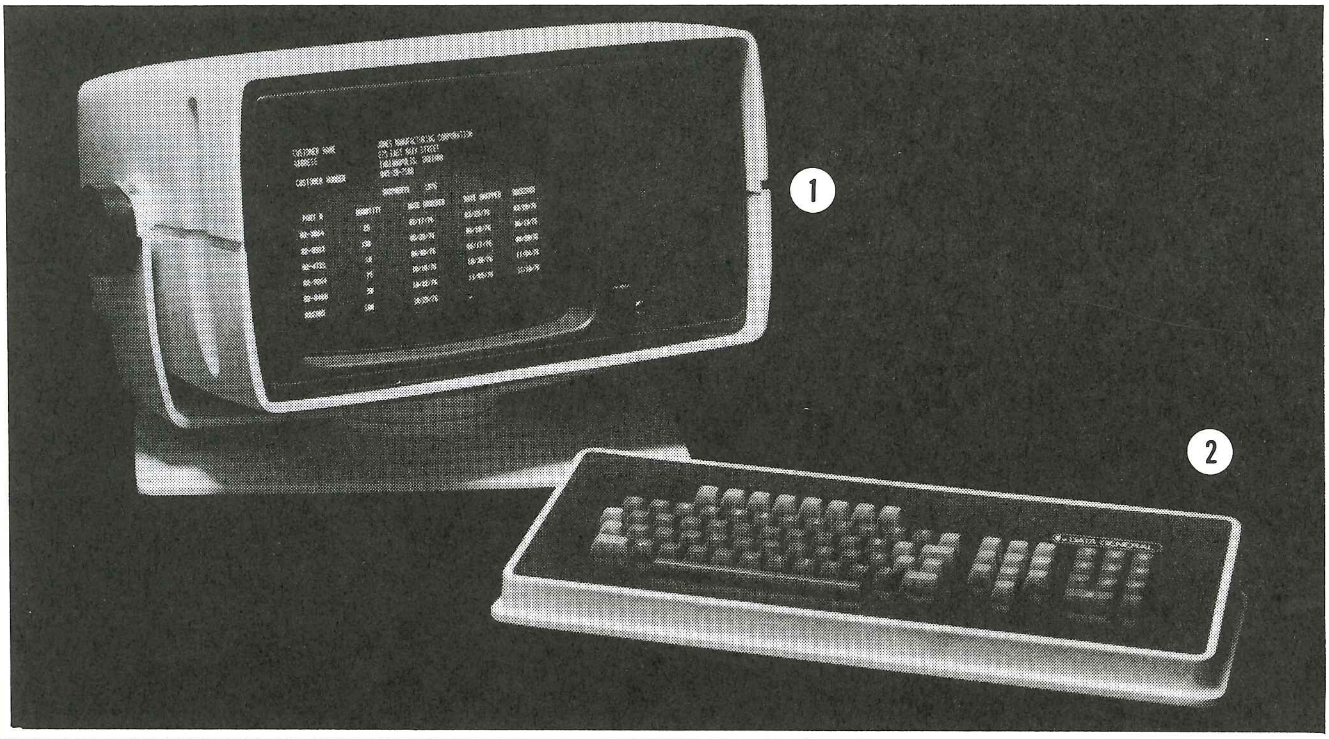
TABLE OF CONTENTS

INTRODUCTION 1
FUNCTIONAL BLOCK DIAGRAM 3
SPECIFICATIONS 4
RELATED DOCUMENTS 5
THEORY OF LOGICAL OPERATION 6
ASYNCHRONOUS INTERFACE BLOCK DIAGRAM 9
DATA RATE TIMING DIAGRAM 10
U/ART CHIP DESCRIPTION 11
CONTROL LOGIC BLOCK DIAGRAM 12
BASIC MEMORY BOARD BLOCK DIAGRAM 14
MEMORY OPTION BLOCK DIAGRAM 15
MEMORY TIMING DIAGRAM 16
DESCRIPTION OF 2K DYNAMIC RAM 17
VIDEO TIMING GENERATOR BLOCK DIAGRAM 18
VIDEO TIMING DIAGRAM 19
VIDEO CHARACTER GENERATOR BLOCK DIAGRAM 20
POWER SUPPLY BLOCK DIAGRAM 21
ASCII CHARACTER SET WITH DISPLAY TERMINAL, MODELS 6052 AND 6053, CONTROL CODES 22
COMPONENTS GUIDE SUPPLEMENT 23

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

This page intentionally left blank.

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.



	COMPONENT
1.	CRT Display, Models 6052, 6053
2.	Keyboard, Model 6052 Keyboard, Model 6053 not shown

MOUNTING
Tabletop

INTRODUCTION

Data General's display terminals, models 6052 and 6053, are soft-copy, full-duplex, I/O devices designed for use in a wide range of interactive terminal applications. The model 6052 is the upper case ASCII, basic terminal; the model 6053 is the full upper/lower case ASCII, enhanced terminal.

Each terminal consists of two units, a CRT display mounted on a fully articulated base and a separate solid state, capacitive switching keyboard, which are connected by a 4 foot, plug-in, external cable. These units function as separate devices, utilizing a common asynchronous interface housed in the display chassis to communicate with the computer. The keyboard is a transmit-only device while the display is a receive-only device with the additional capability of transmitting cursor position information on program request.

The terminal communicates with the computer via either a 20mA current loop or an EIA RS-232C line at switch selectable data rates ranging from 110 baud to 19.2 Kbaud with switch selectable even, odd, or mark parity.

The display unit has a 1920-character, dynamic RAM memory. Each character stored in this memory is displayed as a 5x7 or 5x8 (lower case, model 6053 only) dot matrix on a non-interlaced video monitor with a 12 inch diagonal screen. This screen has an active area of 8.5 inches by 5.5 inches, formatted as 24 lines, 80 characters per line. Characters stored in memory can be blinked, dimmed (model 6053 only) and/or underscored (model 6053 only) on a character by character basis. The cursor is displayed as a blinking underscore. On program command, the screen can be rolled upward one line each time the cursor overflows the bottom line or a New Line code is received when the cursor is on the bottom line.

The keyboards of the two models are different. The basic terminal has a teletypewriter style main keypad while the enhanced terminal has an office typewriter style main keypad. Both keyboards contain three supplementary keypads: an 11-key numeric keypad to facilitate entry of numeric data, a 10 or 12-key (model 6053 only) screen management keypad, and an 8 or 11-key (model 6053 only) user function keypad. The user function keypads expand the capabilities of the terminal by providing the programmer with an additional 32 or 44 (model 6053 only) user-designated codes with which to implement his application.

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

ARCHITECTURE

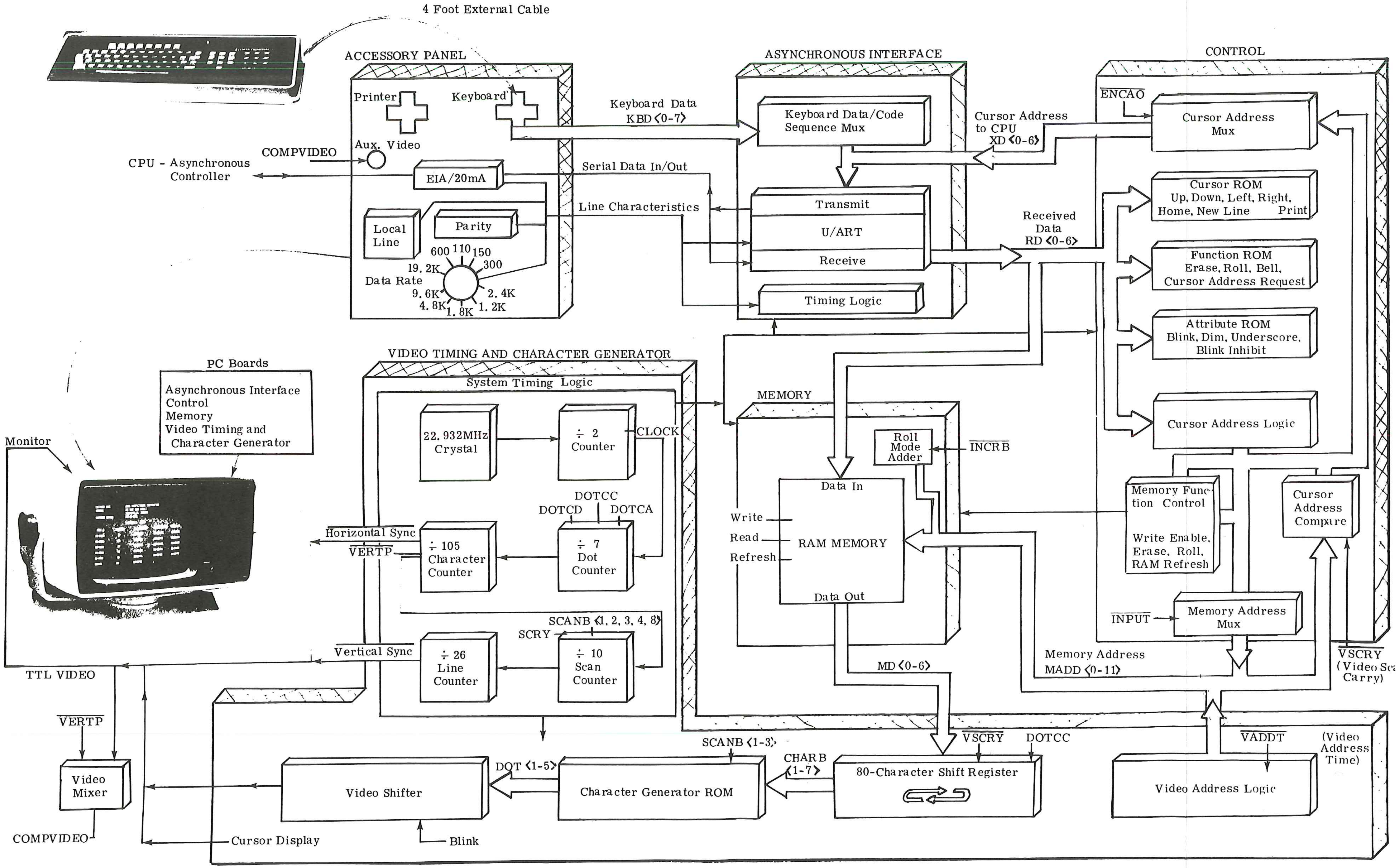
The display terminals incorporate a modular design which facilitates maintenance and provides high reliability. This modularity allows the basic terminal to be easily enhanced.

Each terminal consists of the following main assemblies:

- A keyboard, either the teletypewriter style model 6052 or the office typewriter style model 6053, and an external cable which links the keyboard to the display's asynchronous interface via the accessory panel at the rear of the display unit.
- A CRT display, consisting of the following subassemblies:
    - An accessory panel which contains a receptacle for the keyboard external cable, a data rate rotary switch, a parity slide switch, an online/local mode slide switch, interface connections for a 20mA current loop, an EIA RS-232C line, a printer, and a composite video output jack.
    - A power supply which provides power for the unit.
    - A video monitor which displays the information stored in the memory.
    - An asynchronous interface which forms the communications link between the keyboard, the computer, and the display.
    - Control logic, which decodes the information received from the asynchronous interface, controls the information written into memory, sets blink, dim and underscore bits, and maintains the cursor and memory addresses.
    - A video timing and character generator which provides the system timing for the display and generates the signals necessary to display the alphanumeric characters on the screen of the video monitor.
    - A memory, which stores the information received from the asynchronous interface when instructed to do so by the control logic and passes the information to the video character generator, one line at a time, when instructed to do so by the video timing generator.

The interconnection and primary functions of the above modules, with the exception of the power supply, are shown on the functional block diagram.

FUNCTIONAL BLOCK DIAGRAM



Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

THE 6052, 6053 DISPLAY TERMINAL SPECIFICATIONS

PROPERTIES

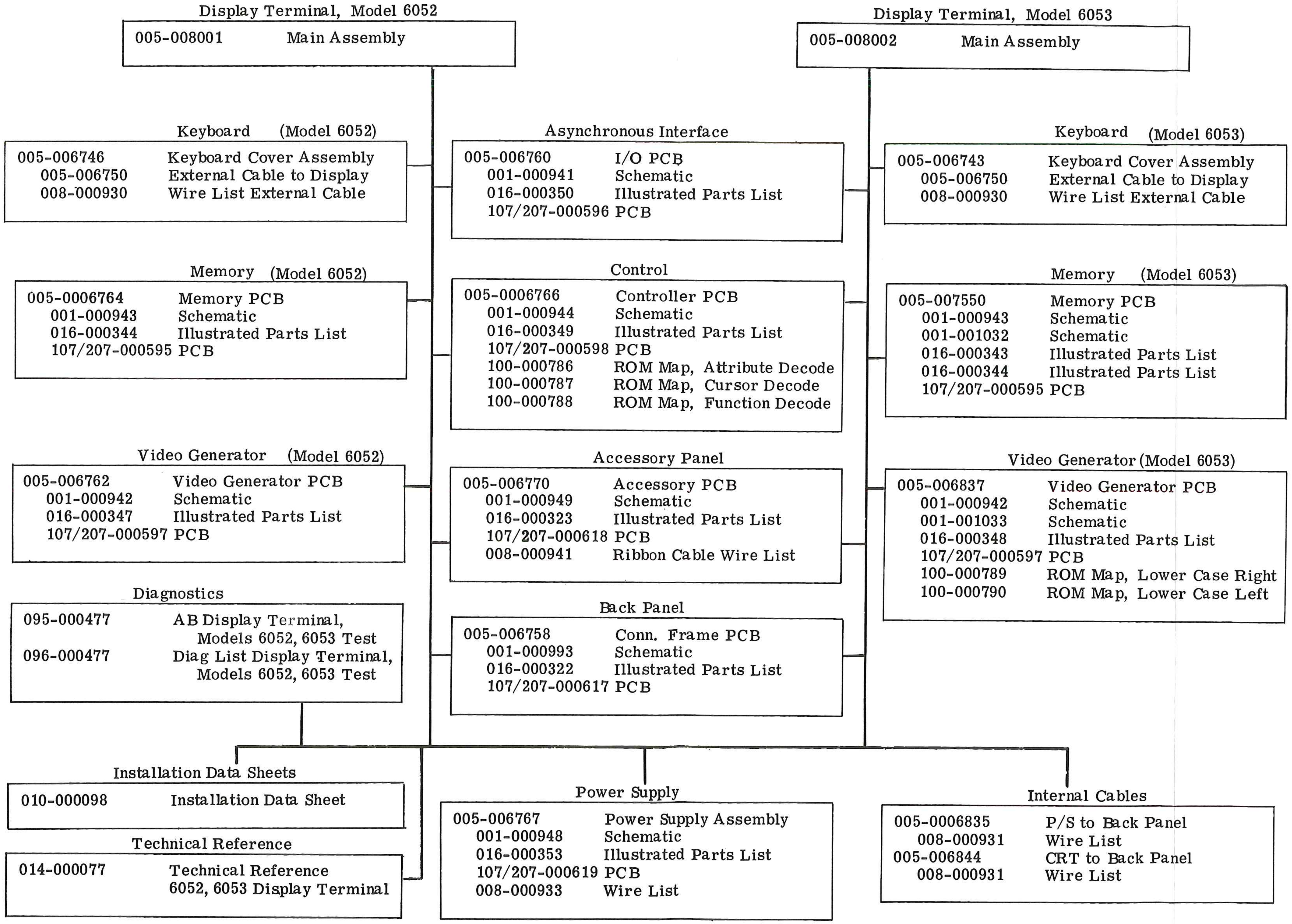
Mounting	Tabletop Display dimensions: 12.5″ X 14.5″ X 20.5″ Keyboard dimensions: 2.75″ X 9″ X 20″
Weight	Display: 45 pounds Keyboard: 7 pounds
Operating Temperature	0 degC to 45 degC
Relative Humidity Range	10% to 95%, non-condensing, operating
Operating Altitude	10,000 feet maximum
Power Requirements	Single Phase, 120Volts, 60Hz (±2Hz) 100Volts, 50Hz (±2Hz) 240Volts, 50Hz (±2Hz) 220Volts, 50Hz (±2Hz)

SYSTEM CAPACITY

Number of displays/system	Depends on controller
Display Information Capacity	1920 characters, formatted as 24 lines, 80 characters/line in a viewing area of 8.5 inches by 5.5 inches on a CRT screen.

CHARACTERISTICS

Data Transmission Mode	Full-duplex	
Data Transmission Type	Asynchronous	
Code Format	ASCII, 10 or 11-bit, serial	
Parity	Even, odd or mark, switch selectable	
Data Rate	110 to 19.2K baud, switch selectable	
Interface	20mA/EIA RS-232C (depending on cable)	
Keyboard	Model 6052	Model 6053
Main keypad style	Teletypewriter style with 4-foot external, plug-in cable to display	Typewriter stye, with 4 foot external, plug-in cable to display
Type	Solid state capacitive switching	
Numeric keypad	11	11
Screen management keypad keys	10	12
User function keypad keys	08	11
Character Set	Model 6052	Model 6053
	ASCII 64 upper case alphanumeric	ASCII 96 upper and lower case alphanumeric
International Fonts	U.K., German, Swedish, French	
Display		
Program addressable cursor	Read current cursor address or send new cursor position	
Blink	Character by character	
Underscore	Model 6053 only, character by character	
Dim	Model 6053 only, character by character	
Roll Screen Enable	Program selectable	
Video Monitor		
Type	Cathode Ray Tube	
Screen size	8.5 inches by 5.5 inches viewing area; 12 inches diagonal	
Character style	Model 6052: 5 X 7 dot matrix Model 6053: 5 X 8 dot matrix	
Display	Non-interlaced raster scan	
Phosphor	P4 White	
Deflection	Magnetic	
Focus	Dynamic and static	



Display Terminal, Model 6052

005-008001	Main Assembly

Display Terminal, Model 6053

005-008002	Main Assembly

Keyboard (Model 6052)

005-006746	Keyboard Cover Assembly
005-006750	External Cable to Display
008-000930	Wire List External Cable

Asynchronous Interface

005-006760	I/O PCB
001-000941	Schematic
016-000350	Illustrated Parts List
107/207-000596	PCB

Keyboard (Model 6053)

005-006743	Keyboard Cover Assembly
005-006750	External Cable to Display
008-000930	Wire List External Cable

Memory (Model 6052)

005-0006764	Memory PCB
001-000943	Schematic
016-000344	Illustrated Parts List
107/207-000595	PCB

Control

005-0006766	Controller PCB
001-000944	Schematic
016-000349	Illustrated Parts List
107/207-000598	PCB
100-000786	ROM Map, Attribute Decode
100-000787	ROM Map, Cursor Decode
100-000788	ROM Map, Function Decode

Memory (Model 6053)

005-007550	Memory PCB
001-000943	Schematic
001-001032	Schematic
016-000343	Illustrated Parts List
016-000344	Illustrated Parts List
107/207-000595	PCB

Video Generator (Model 6052)

005-006762	Video Generator PCB
001-000942	Schematic
016-000347	Illustrated Parts List
107/207-000597	PCB

Accessory Panel

005-006770	Accessory PCB
001-000949	Schematic
016-000323	Illustrated Parts List
107/207-000618	PCB
008-000941	Ribbon Cable Wire List

Video Generator (Model 6053)

005-006837	Video Generator PCB
001-000942	Schematic
001-001033	Schematic
016-000348	Illustrated Parts List
107/207-000597	PCB
100-000789	ROM Map, Lower Case Right
100-000790	ROM Map, Lower Case Left

Diagnostics

095-000477	AB Display Terminal, Models 6052, 6053 Test
096-000477	Diag List Display Terminal, Models 6052, 6053 Test

Back Panel

005-006758	Conn. Frame PCB
001-000993	Schematic
016-000322	Illustrated Parts List
107/207-000617	PCB

Installation Data Sheets

010-000098	Installation Data Sheet

Technical Reference

014-000077	Technical Reference 6052, 6053 Display Terminal

Power Supply

005-006767	Power Supply Assembly
001-000948	Schematic
016-000353	Illustrated Parts List
107/207-000619	PCB
008-000933	Wire List

Internal Cables

005-0006835	P/S to Back Panel
008-000931	Wire List
005-006844	CRT to Back Panel
008-000931	Wire List

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

THEORY OF LOGICAL OPERATION

INTRODUCTION

The display terminals, models 6052 and 6053, consist of two I O devices, the keyboard as the input device and the display as the output device, and an asynchronous interface which is an integral part of the display unit.

Keyboard

Information is entered in the keyboard by selectively pressing the keys. The keyboard converts each keystroke into an 8-bit ASCII character code and sends this code in parallel form, together with a strobe signal, to the asynchronous interface via the external cable.

Asynchronous Interface

The asynchronous interface tests bit 8 of each keyboard code as it is received to ascertain if it is a user function code. (All user function codes have a 1 in bit 8, KBD7. Refer to the asynchronous interface block diagram.) If it is not a user function code, the remaining seven bits of the code are multiplexed to a U/ART (universal asynchronous transmitter-receiver). If it is a user function code, a user function header code (036_8) is multiplexed to the U/ART followed by the 7-bit keyboard code; thus providing a two-code sequence.

The U/ART adds the start, stop and selected parity bits to each 7-bit character code and transmits a 10-bit or 11-bit (110 baud only) code in serial form to an asynchronous controller in the computer via either a 20mA current loop or an EIA RS-232C communications line.

On receipt of serial information from the computer, the U/ART tests each character code for parity and framing errors, strips the start, stop and parity bits, and converts the seven data bits to parallel form. When the 7-bit code leaves the U/ART the error signals generated by the U/ART are tested. If the code was received error free, it passes to the RD bus. If the code contained an error, a code containing all ones is passed to the RD bus. (A parity or framing error causes a question mark, 077_8, to be displayed on the screen of the basic terminal; it causes a delete or rubout code, 177_8, to be displayed as a 5x7 dot matrix with all dots intensified on the screen of the enhanced terminal.) The RD bus carries the code to the control logic and the memory boards.

Control Logic

The control logic decodes each character to ascertain if it is a displayable,alphanumeric character or if it is a display control character. If it is a displayable character, the control logic generates the signals which allow the code on the RD bus to be written into memory. If it is a display control code, three ROMS (refer to the control logic block diagram) decode the code and generate the appropriate display control signal(s). In addition, the control logic maintains the cursor and memory addresses.

When the read cursor address code (005_8) is decoded, a cursor address request signal is sent to the asynchronous interface. The asynchronous interface multiplexes the cursor address header code (037_8) to the U ART and then disables the multiplexer. During this time, the control logic passes a two-code sequence, consisting of the cursor column address, followed by the cursor row address, to the XD bus. The XD bus carries the codes to the asynchronous interface and the three-code sequence (header code, cursor column address, cursor row address) is sent to the computer.

Memory

The memory board consists of seven (model 6052) or ten (model 6053) 1x2K dynamic RAMs, together with the logic which updates the memory addresses when the roll screen enable bit is set. (Refer to the memory block diagrams, the memory timing diagram and the description of the 2K dynamic RAM.)

During the write cycle, information on the RD bus (on the basic memory board, bit 6 of the code, RD5, is ignored) and the blink, dim (model 6053 only) and underscore (model 6053 only) bits are written into memory by signals generated from the control logic and the video timing generator. (The blink, dim and underscore bits become an integral part of the character code when it is stored in memory.) The memory addresses provided to the RAMs during the write cycle are generated by the control logic.

During the read cycle, memory reading is enabled by signals generated by the video timing and character generator. The memory addresses provided to the RAMs during the read cycle are generated by the video timing generator logic. Information read from memory is sent to the video character generator via the MD bus.

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

Video Timing and Character Generator

A 22.932MHz crystal oscillator in the video timing logic generates the timing signals which control the operation of the display unit. (Refer to the video timing generator block diagram.)

The video control logic generates the horizontal/vertical sync signals sent to the video monitor, together with the cursor blink rate, the character blink rate, and dim signals.

The video control logic also maintains the video column and row addresses and sends these addresses to the memory board, via the MADD bus, at video address time. (Refer to the video timing diagram.)

At video address time, the next line of characters to be displayed on the screen is read from memory and the cursor address in the control logic is tested to determine if the cursor will appear on the next line of characters to be displayed.

Refer to the video character generator block diagram. As the 80 characters read from memory appear on the MD bus, together with their blink, dim (model 6053) and underscore (model 6053) bits, they are loaded into an 80-character recirculating shift register in the video generator logic. The 80 characters stored in this register are read, one scan at a time (refer to the video monitor described later in the text). The output of this register is passed to the dot generator ROM (on the model 6053, there are three ROMs - upper case and left and right lower case). CHARB7 is complemented on the basic terminal board before it is passed to the upper case dot generator ROM; thus providing the space code, 040_8, when the character code contains all zeroes.

The serial output of the dot generator ROM(s) provides the proper signal (TTL VIDEO) to display the character codes as 5x7 or 5x8 (lower case, model 6053) dot matrices on the CRT screen.

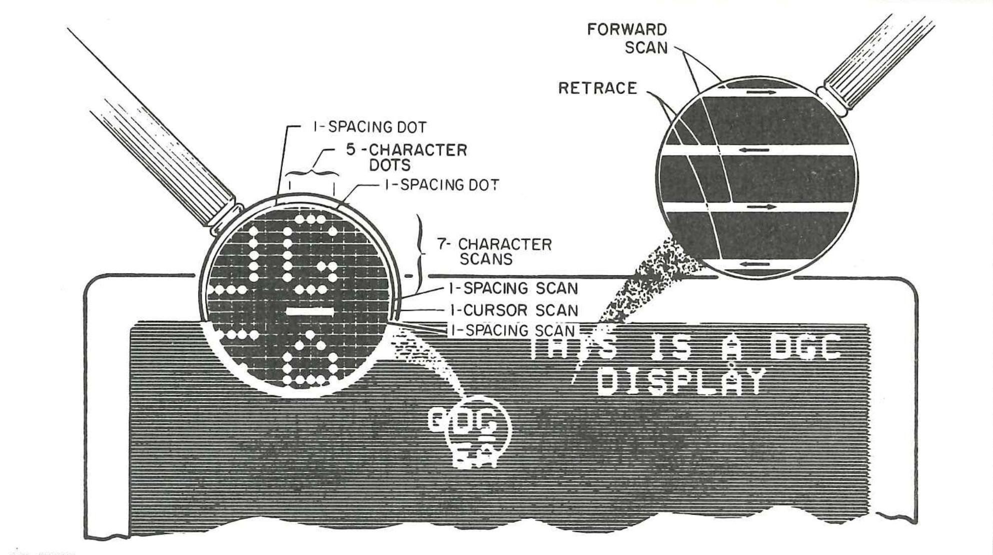
Video Monitor

The video monitor is the display's output, providing a visual image of each character stored in memory on a CRT screen. The monitor uses a pattern of lines traced with an electron beam to display alphanumeric characters as dot matrices.

The monitor is a magnetically deflected device which uses a non-interlaced raster pattern of scanning. A raster is a system of parallel horizontal lines to display characters on the CRT screen. Discrete positions within the raster are defined in the video control logic by a number of parameters, line, scan, character, and dot positions.

The monitor is synchronized by the video control logic and consists of electromagnetic deflection circuits which move the CRT's electron beam horizontally and vertically around the screen. The electron beam scans the screen to display 24 lines of alphanumeric data, 80 characters wide.

There are 24 lines displayed in the screen's active area (8.5 inches by 5.5 inches). It also has spacing for margins at top, bottom and sides. Each line consists of 10 horizontal scans. As the monitor's electron beam makes each horizontal scan, it traces one slice of a line. These scans are divided into 80 character positions across the screen. Each character position is divided into 7 dot positions in which the electron



DG-02006

Note:

During the last spacing scan shown above, the 80-character recirculating shift register is filled with the next line of characters to be displayed.

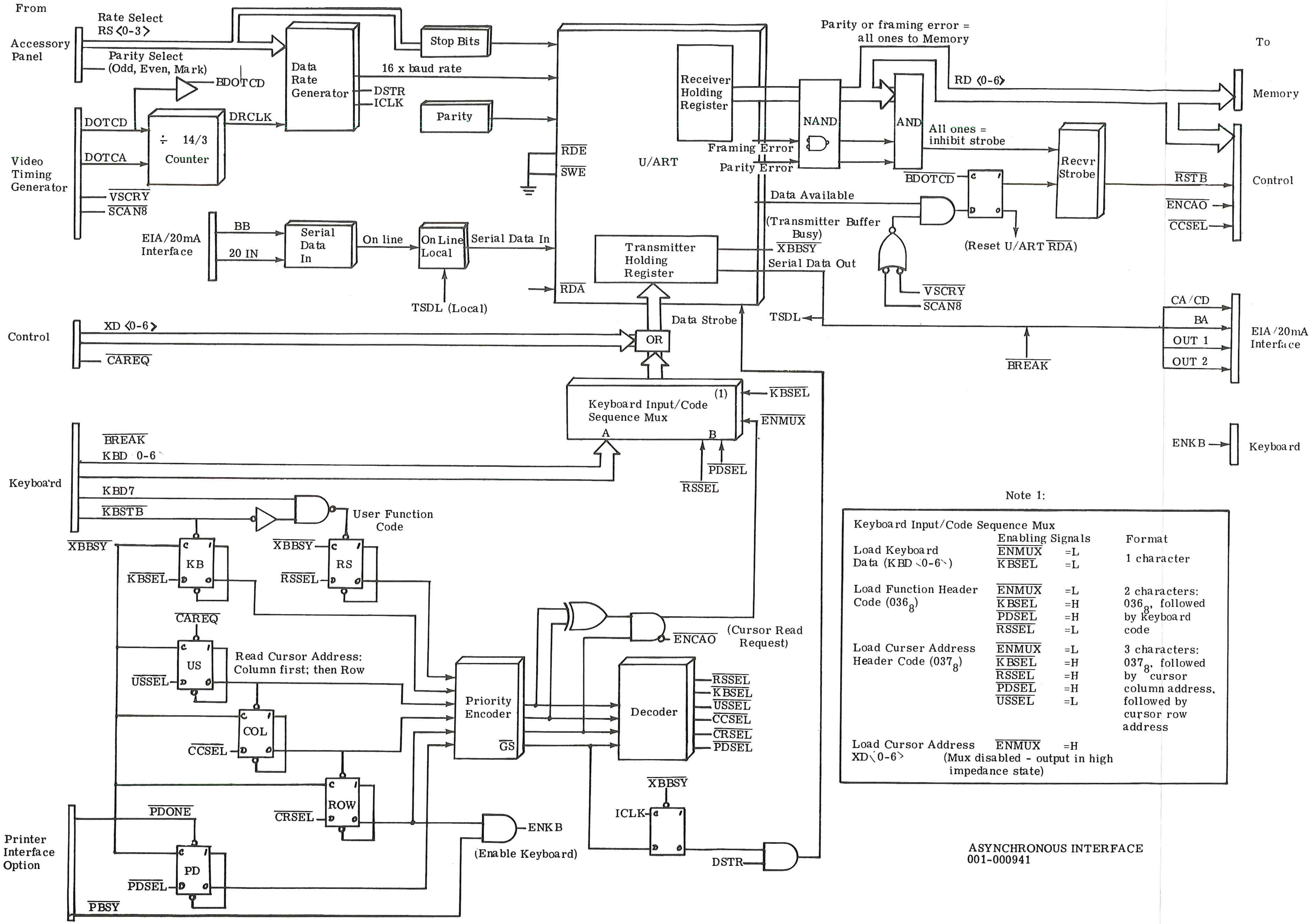
Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

beam may be intensified (unblanked) or held at a low enough intensity so that a visible trace does not appear on the screen (blanked). This scanning produces a character field make up of 7x10 distinct dots. The actual synchronization and control of the raster is external to the monitor, contained in the video control logic.

The monitor's deflection circuits are synchronized and triggered to produce the trace,as shown, by separate signals derived from the video control logic. The horizontal deflection circuit is synchronized to a 15.6KHz signal from the video control, and creates a sawtooth current which drives the electron beam across the screen. The vertical deflection circuit is triggered by a 60Hz or 50Hz signal from the video control logic and creates a current sawtooth which drives the electron beam to the top of the screen. This combination of scanning frequencies produces 260 horizontal scans for each vertical scan.

A detailed description of the monitor, including troubleshooting guides can be found in the vendor supplied instruction manual.

ASYNCHRONOUS INTERFACE
Block Diagram



Note 1:

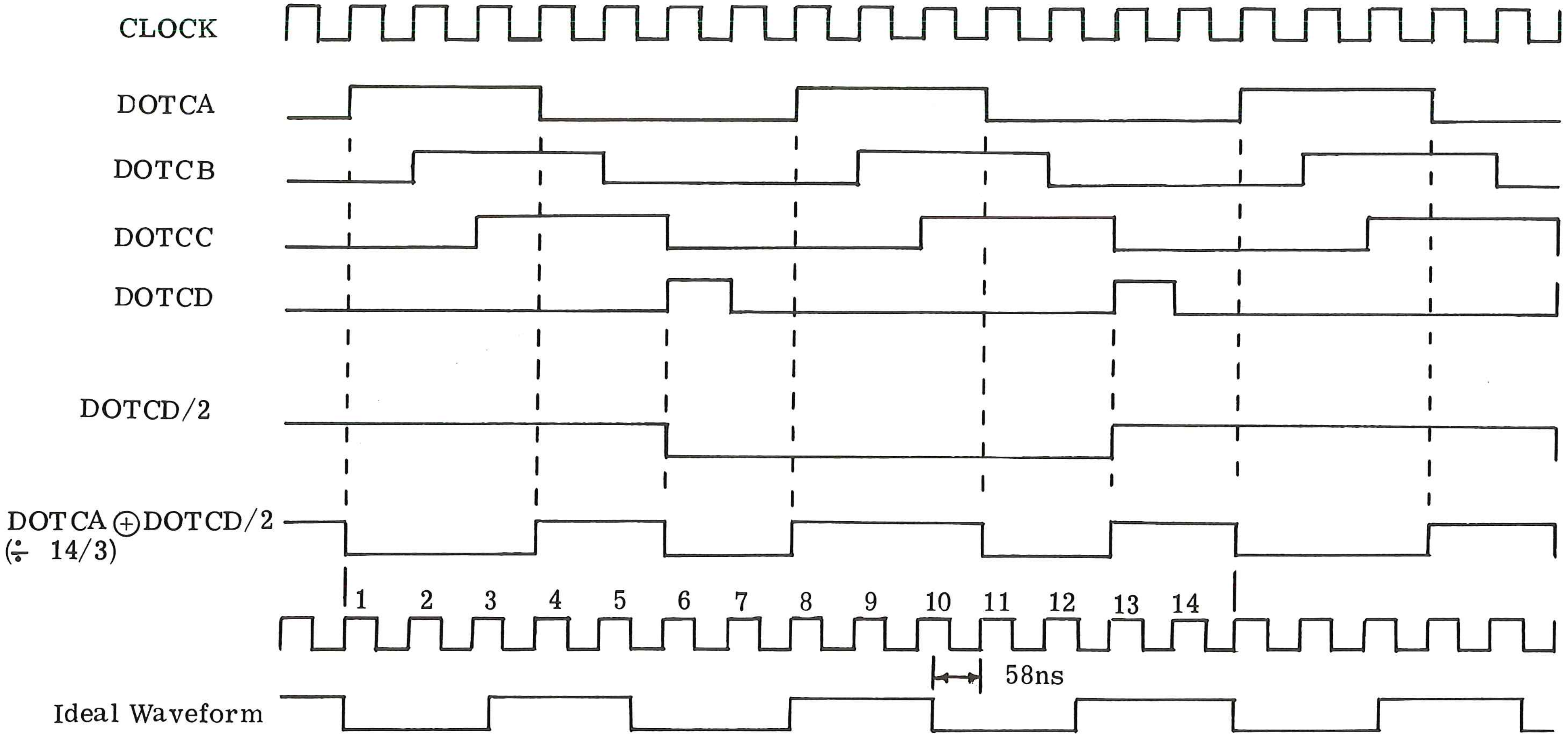
Keyboard Input/Code Sequence Mux

	Enabling Signals		Format
Load Keyboard Data (KBD ⟨0-6⟩)	$\overline{\mathrm{ENMUX}}$ $\overline{\mathrm{KBSEL}}$	=L =L	1 character
Load Function Header Code (036_8)	$\overline{\mathrm{ENMUX}}$ $\overline{\mathrm{KBSEL}}$ $\overline{\mathrm{PDSEL}}$ $\overline{\mathrm{RSSEL}}$	=L =H =H =L	2 characters: 036_8, followed by keyboard code
Load Curser Address Header Code (037_8)	$\overline{\mathrm{ENMUX}}$ $\overline{\mathrm{KBSEL}}$ $\overline{\mathrm{RSSEL}}$ $\overline{\mathrm{PDSEL}}$ $\overline{\mathrm{USSEL}}$	=L =H =H =H =L	3 characters: 037_8, followed by cursor column address, followed by cursor row address
Load Cursor Address XD⟨0-6⟩	$\overline{\mathrm{ENMUX}}$ (Mux disabled - output in high impedance state)	=H	

ASYNCHRONOUS INTERFACE
001-000941

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

DATA RATE TIMING



Design frequency = 2.4576MHz

Actual frequency = 11.466 x 3/14 = 2.457MHz Δ = -.024%

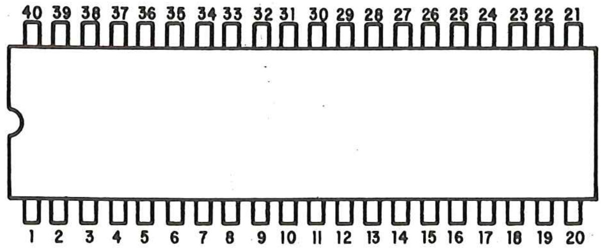
Max. instantaneous error = -(.024% + 58ns)

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

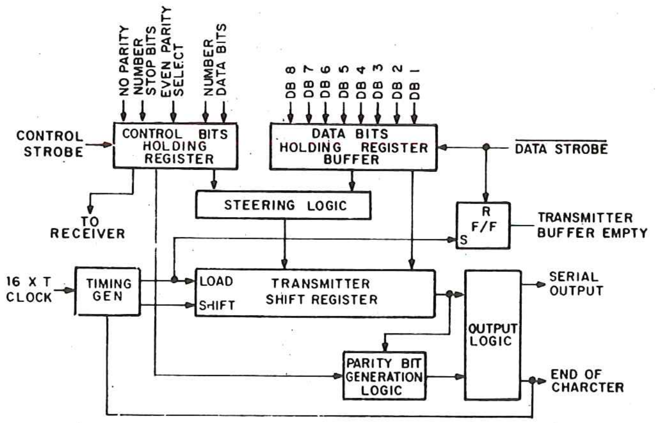
U/ART

The Asynchronous Receiver/Transmitter is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits and either odd/even parity or no parity. The baud rate (bits per word), parity mode and the number of stop bits are externally selectable.

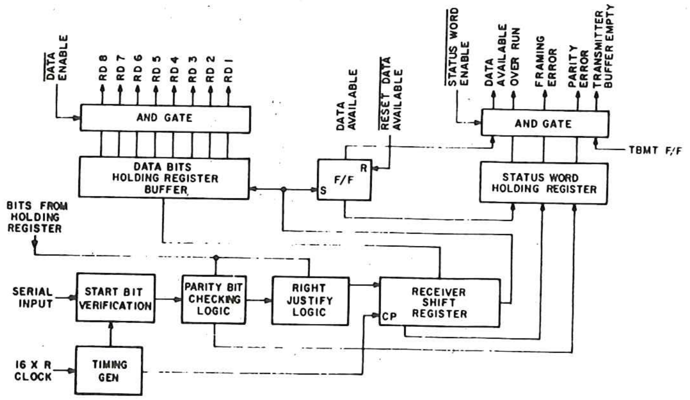
Pin Configuration



Transmitter Block Diagram



Receiver Block Diagram

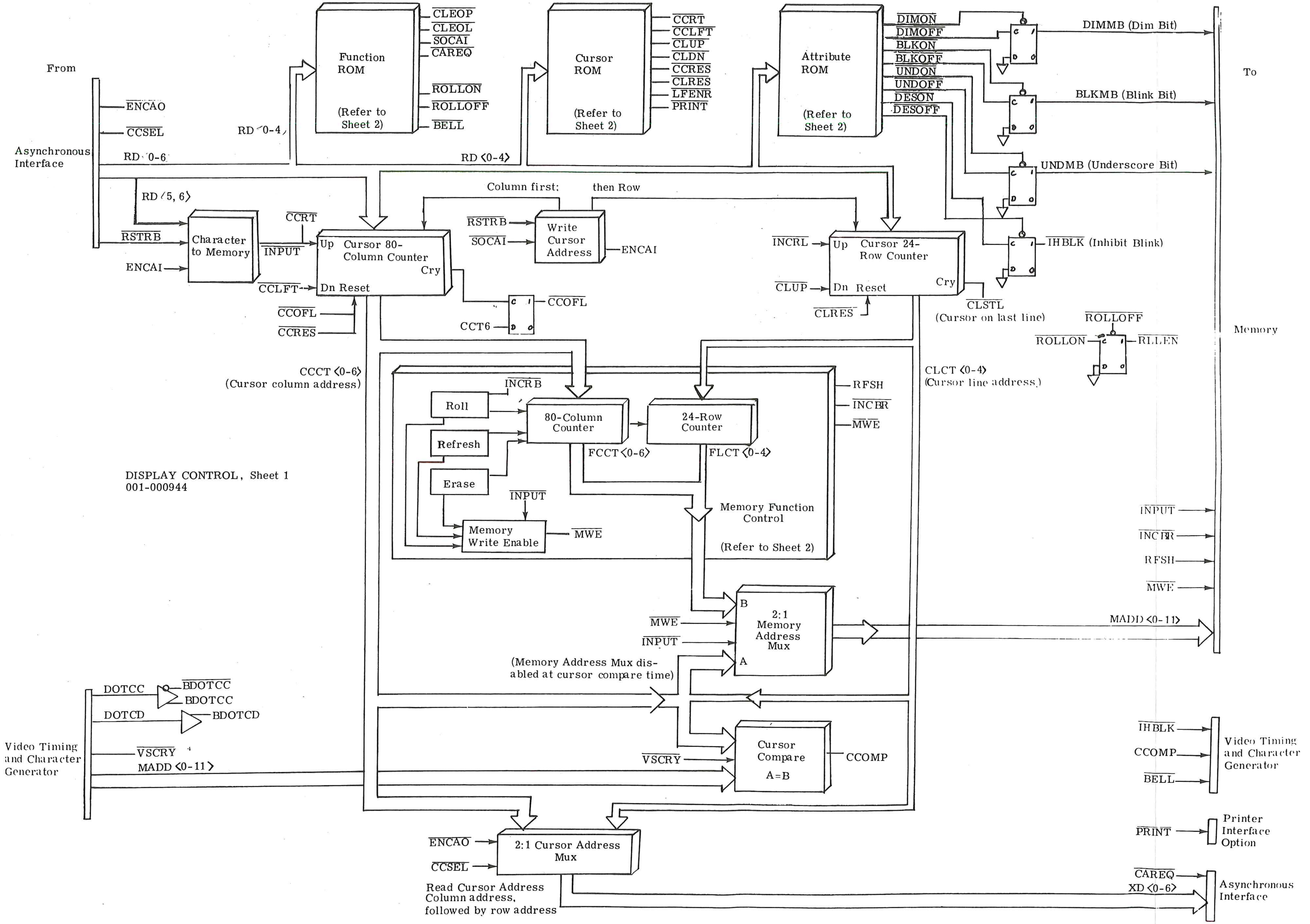


Description of Pin Functions

Pin No.	Name	Symbol	Function
1	V_{cc} Power Supply	V_{cc}	+5V Supply
2	V_{gg} Power Supply	V_{gg}	-12V Supply
3	Ground	V_{gr}	Ground
4	Received Data Enable	$\overline{\text{RDE}}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented.
13	Receive Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected POE.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit.
15	Over-Run	OR	This line goes to a logic "1" if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver holding register.
16	Status Word Enable	$\overline{\text{SWE}}$	A logic "0" on this line places the status word bits (PE, FE, OR, DA, TBMT) onto the output lines. These are tri-state also.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data Available	$\overline{\text{RDA}}$	A logic "0" will reset the DA line.
19	Receive Data Available	DA	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception.
21	External Reset	XR	Resets all registers. Sets SO, EOC, and TBMT to a logic "1".
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character.
23	Data Strobe	$\overline{\text{DS}}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character.
25	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.
26-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
34	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits character. NB1 NB2 Bits Character 0 0 5 1 0 6 0 1 7 1 1 8
39	Odd Even Parity	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock Line	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

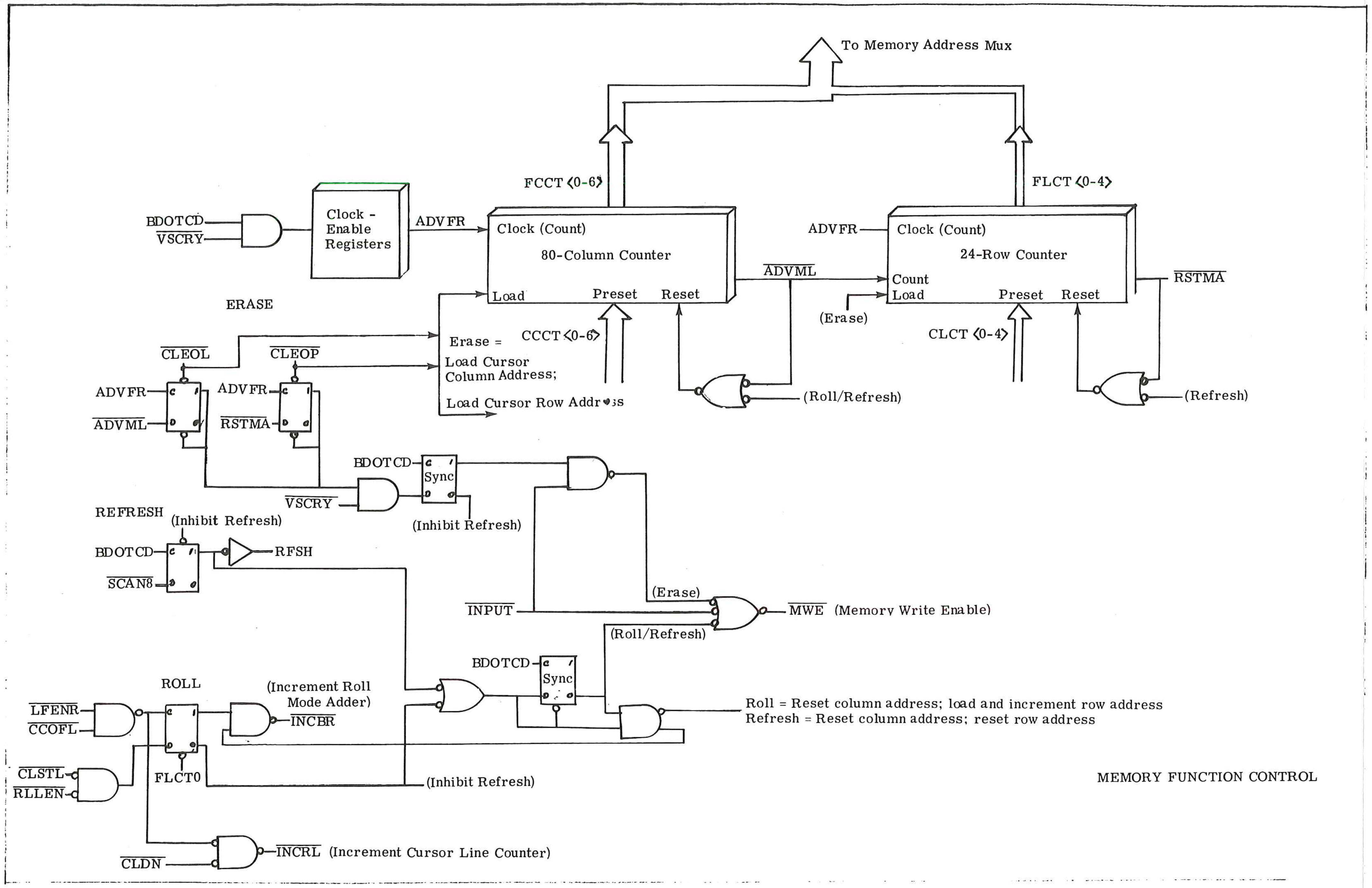
Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

CONTROL LOGIC
Block Diagram, Sheet 1



Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

CONTROL LOGIC
Block Diagram, Sheet 2



DISPLAY CONTROL, Sheet 2
001-000944

ROM DECODES

Function ROM

ROM Address	Code	Function
023	014	EOP (Erase page)
024	013	EOL (Erase to end of line)
017	020	SOCAI (Write cursor address)
032	005	CAREQ (Read cursor address)
015	022	ROLLON (Enable Roll mode)
014	023	ROLLOFF (Disable Roll mode)
030	007	BELL (Bell)

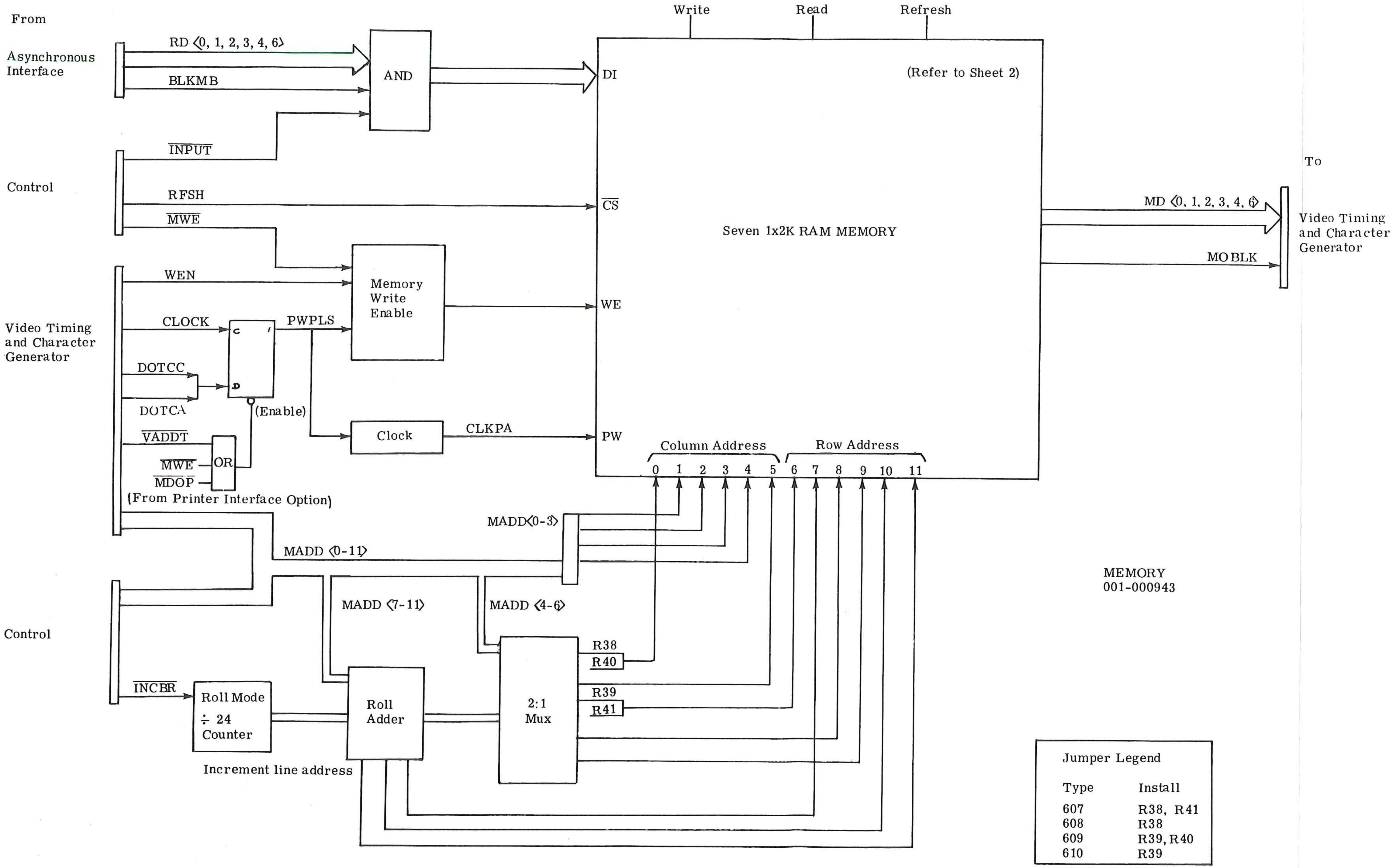
Cursor ROM

ROM Address	Code	Function
007	030	CCRT(Cursor right)
006	031	CCLFT (Cursor left)
010	027	CLUP (Cursor up)
005	032	CLDN (Cursor down)
022	015	CCRES (Return)
027	010	CLRES (Home)
025	012	LFENR (New Line)
016	021	PRINT (Print)

Attribute ROM

ROM Address	Code	Function
003	034	DIMON (Dim on)
002	035	DIMOFF (Dim off)
021	016	BLKON (Blink on)
020	017	BLKOFF (Blink off)
013	024	UNDON (Underscore on)
012	025	UNDOFF (Underscore off)
034	003	DESON (Enable blink)
033	004	DESOFF (Inhibit blink)

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.



MEMORY
001-000943

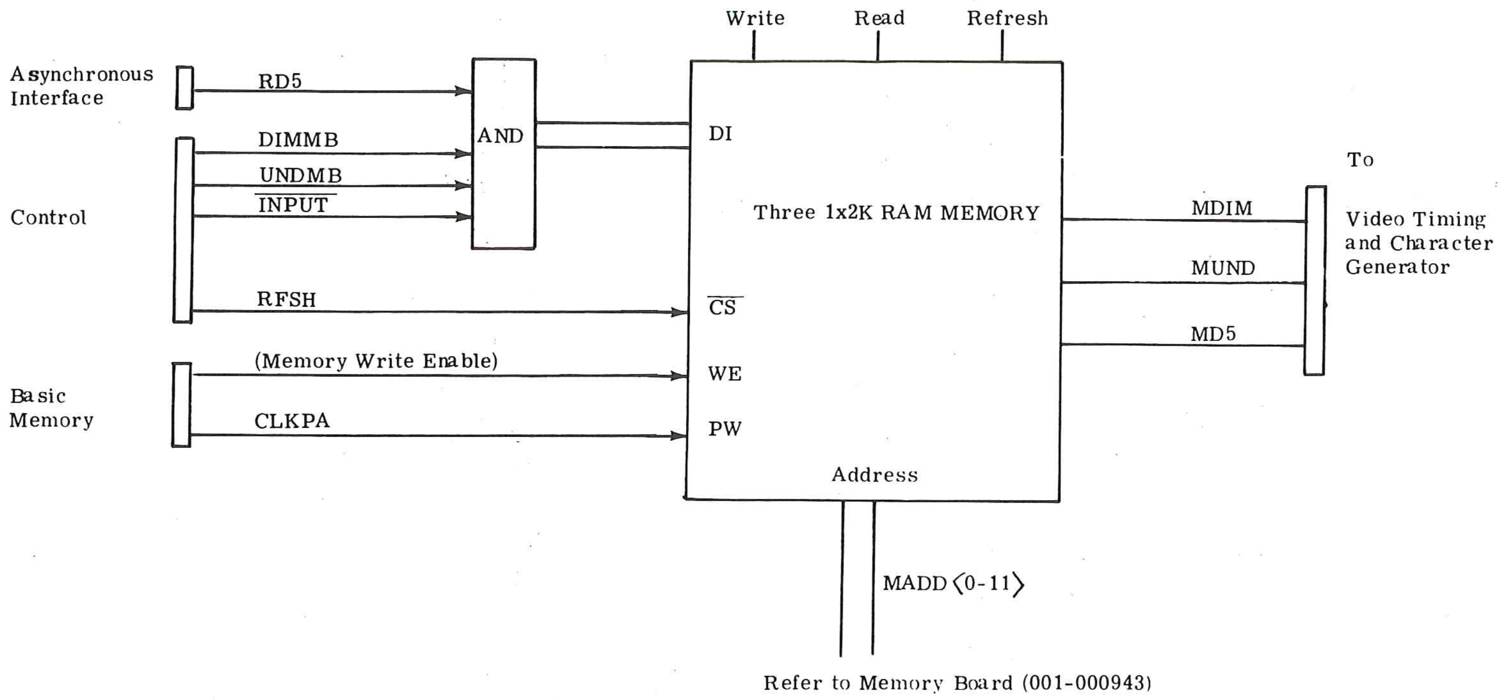
Jumper Legend

Type	Install
607	R38, R41
608	R38
609	R39, R40
610	R39

(Refer to Sheet 2)

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

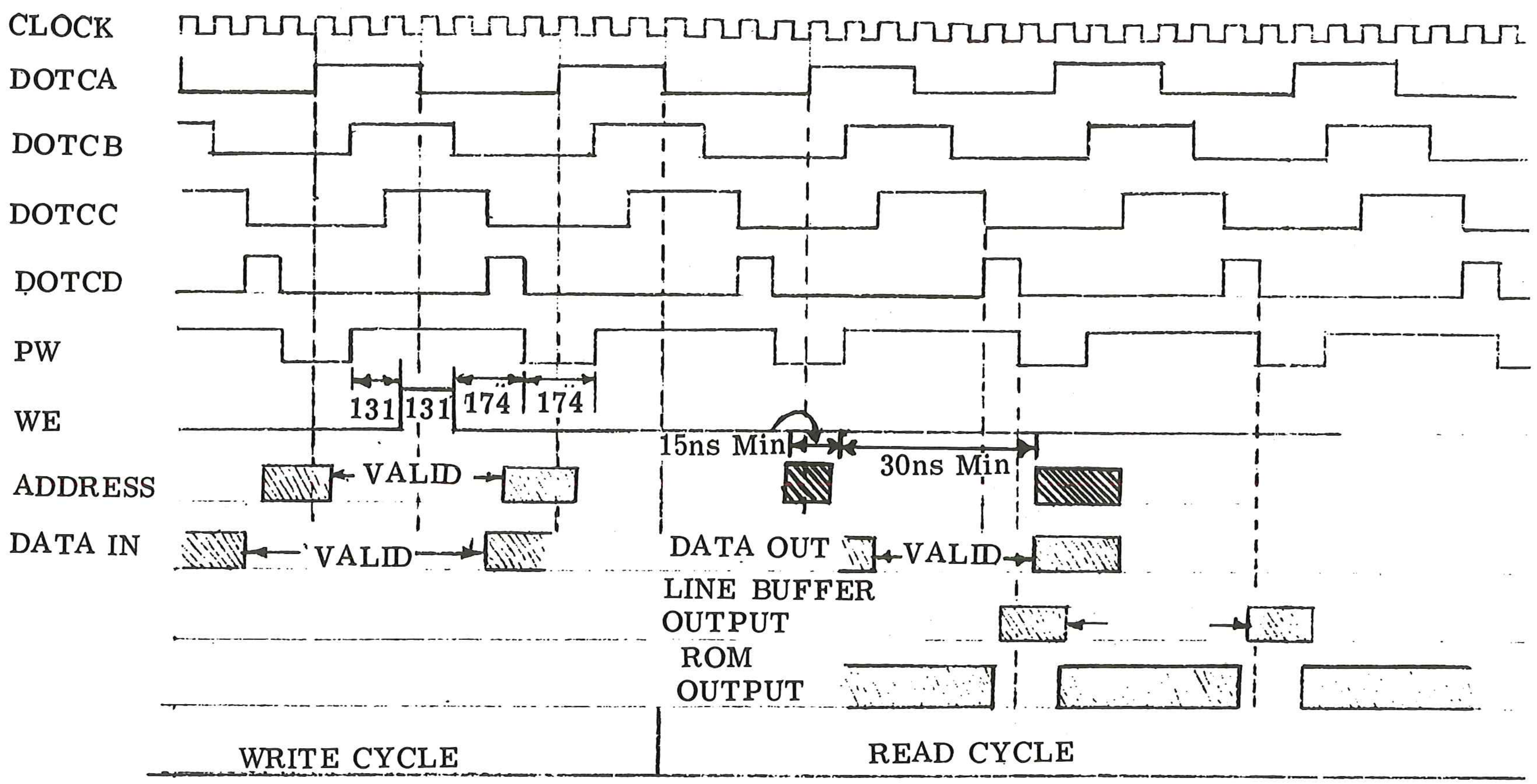
MEMORY
Block Diagram, Memory Option



MEMORY OPTION
TERMINAL ENHANCEMENT
001-001032

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide in the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

MEMORY TIMING



Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

FUNCTIONAL DESCRIPTION

The 2K dynamic RAM is a 2048-bit dynamic random-access memory. It reads and writes each bit individually and refreshes sixty-four bits simultaneously.

Pins

The pins of the memory and brief descriptions of their functions are given in the following table.

Pin	function
P	clock input
$\overline{CS}$	chip select
WE	write-enable
A[0-11]	address inputs
D/O	data output
D/I	data input

Memory Operations

A memory operation is initiated when P goes to high level. At this time, the address on A[0-11] is sampled. A change in the electrical levels of these pins after they are sampled does not affect the operation of the RAM.

The operation that the RAM performs depends on the level at $\overline{CS}$ at the time P rises. If $\overline{CS}$ is low, a read operation is initiated. The address sampled on the rising edge of P selects one data bit in the memory. Soon after the address is sampled, D/O assumes the low state and then assumes the high state or the low state as required to reflect the contents of the selected data bit.

Once a read operation is initiated, it may be converted to a read followed by a write by a high level at WE. A rising edge of WE places D/O in the high state. A falling edge of WE loads the selected data bit from D/I. D/I and D/O have the opposite sense; that is, if D/I is at high level when a data bit is loaded, D/O assumes the low state when the data bit is read.

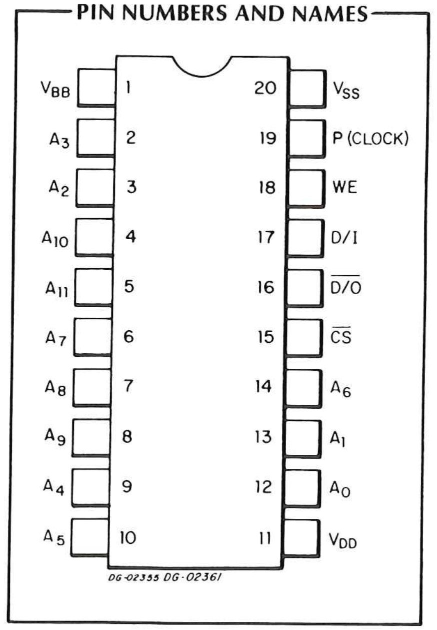
When P rises and $\overline{CS}$ is high, a refresh operation is initiated. The address sampled on the rising edge of P selects sixty-four data bits in the memory. D/O remains in the high impedance state for the duration of the memory refresh operation.

Once a refresh operation is initiated, WE determines whether or not the sixty-four selected data bits are refreshed. A falling edge of WE refreshes the selected data bits. A bit is refreshed if the address bits most recently latched from [A 6-11] are identical to the address bits that would be latched from A[6-11] in order to select the bit for reading or writing. The contents of every bit remain unchanged during a refresh operation; no bit is loaded from D/I.

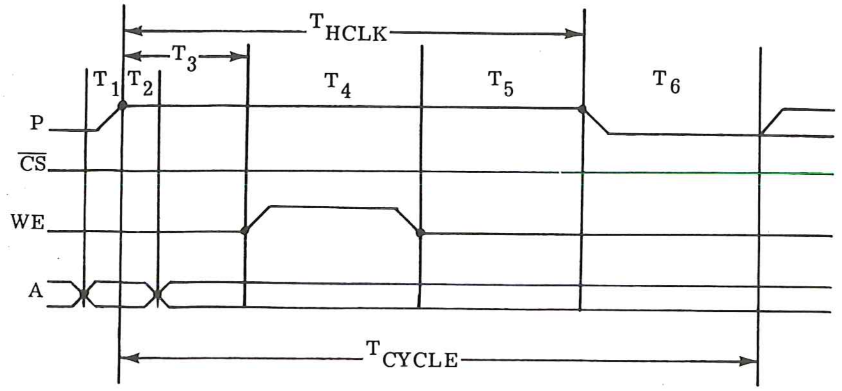
The memory operation is concluded when P goes to low level. After a read operation, the falling edge of P may occur as soon as the data has been read. After a write or refresh operation, there is a minimum delay between the falling edges of WE and P. There is also a minimum delay between the falling edge of P that concludes a memory operation and the rising edge of P that initiates the next one.

The following timing diagrams depict the events that occur on the pins of the RAM during the memory operations described above.

PIN NUMBERS AND NAMES

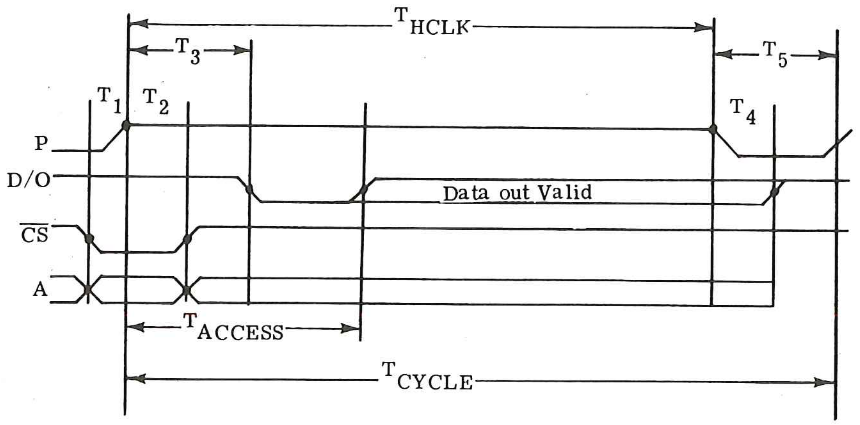


REFRESH OPERATION



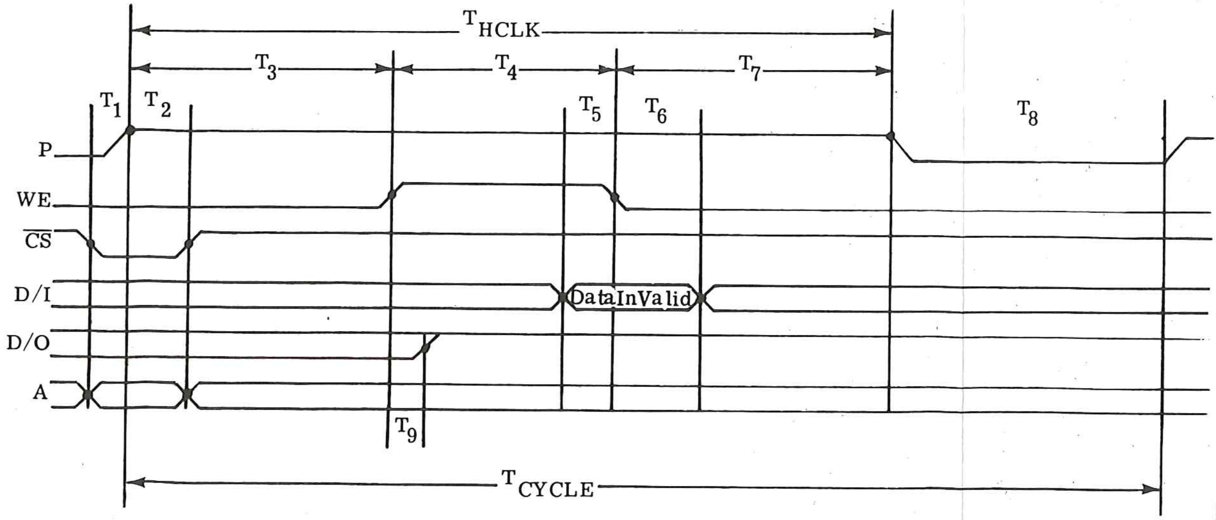
	MIN (ns)	MAX (ns)
T_1	20	-
T_2	30	-
T_3	120	-
T_4	130	-
T_5	130	-
T_6	140	-
T_{HCLK}	400	2000
T_{CYCLE}	515	2.4ms

READ OPERATION



	MIN (ns)	MAX (ns)
T_1	15	-
T_2	30	-
T_3	-	55
T_4	0	-
T_5	145	-
T_{ACCESS}	-	160
T_{HCLK}	-	2000
T_{CYCLE}	285	2.4ms

WRITE OPERATION

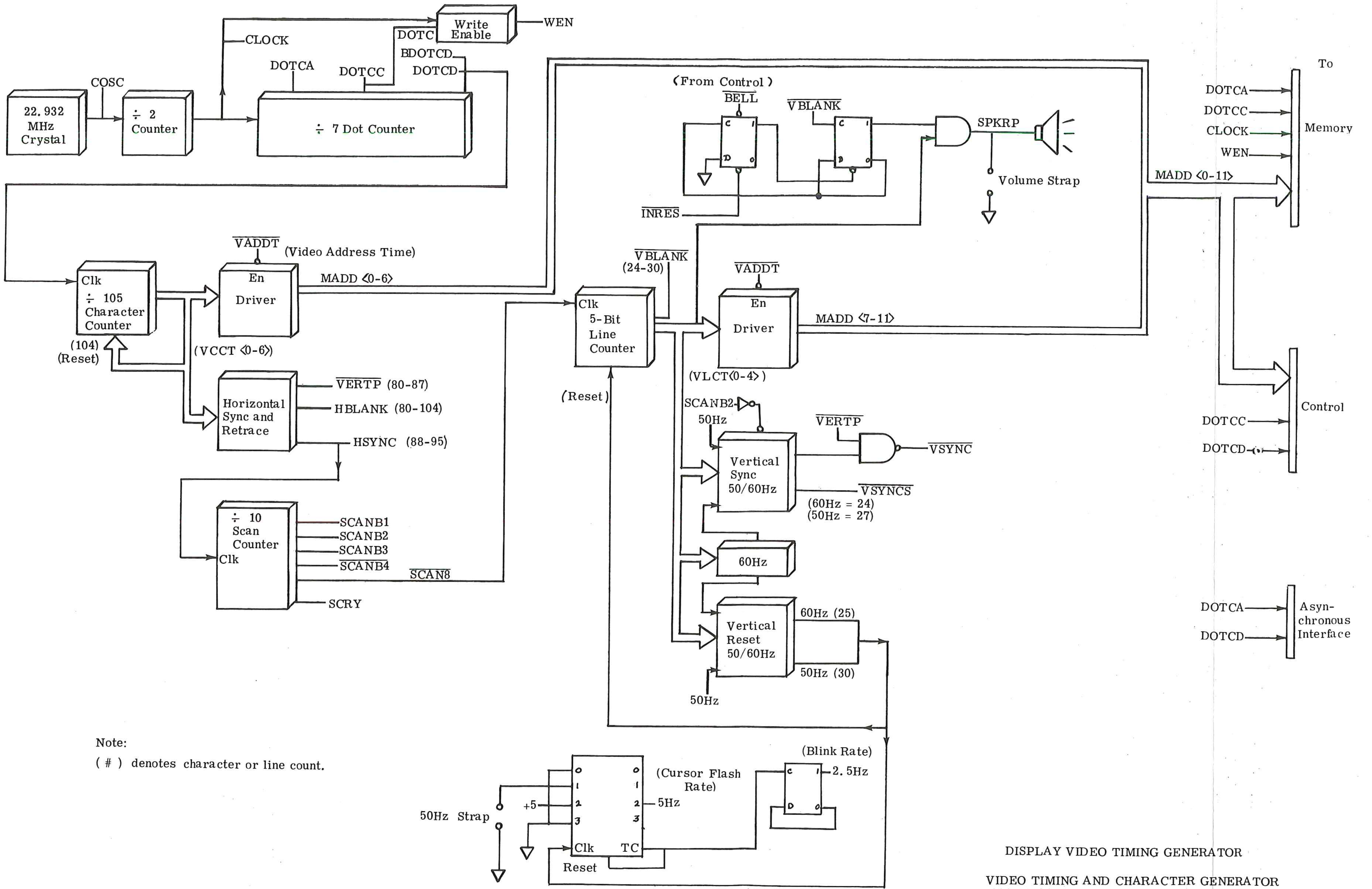


	MIN (ns)	MAX (ns)
T_1	15	-
T_2	30	-
T_3	135	-
T_4	145	-
T_5	35	-
T_6	55	-
T_7	145	-
T_8	145	-
T_9	25	-
T_{HCLK}	-	2000
T_{CYCLE}	570	2.4ms

P(CLOCK)	Input Rise Time	10 to 20ns
P(CLOCK)	Input Fall Time	10 to 20ns
All Other	Input Fall Times	5 to 15ns
All Other	Input Rise Times	5 to 15ns

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

VIDEO TIMING GENERATOR
Block Diagram



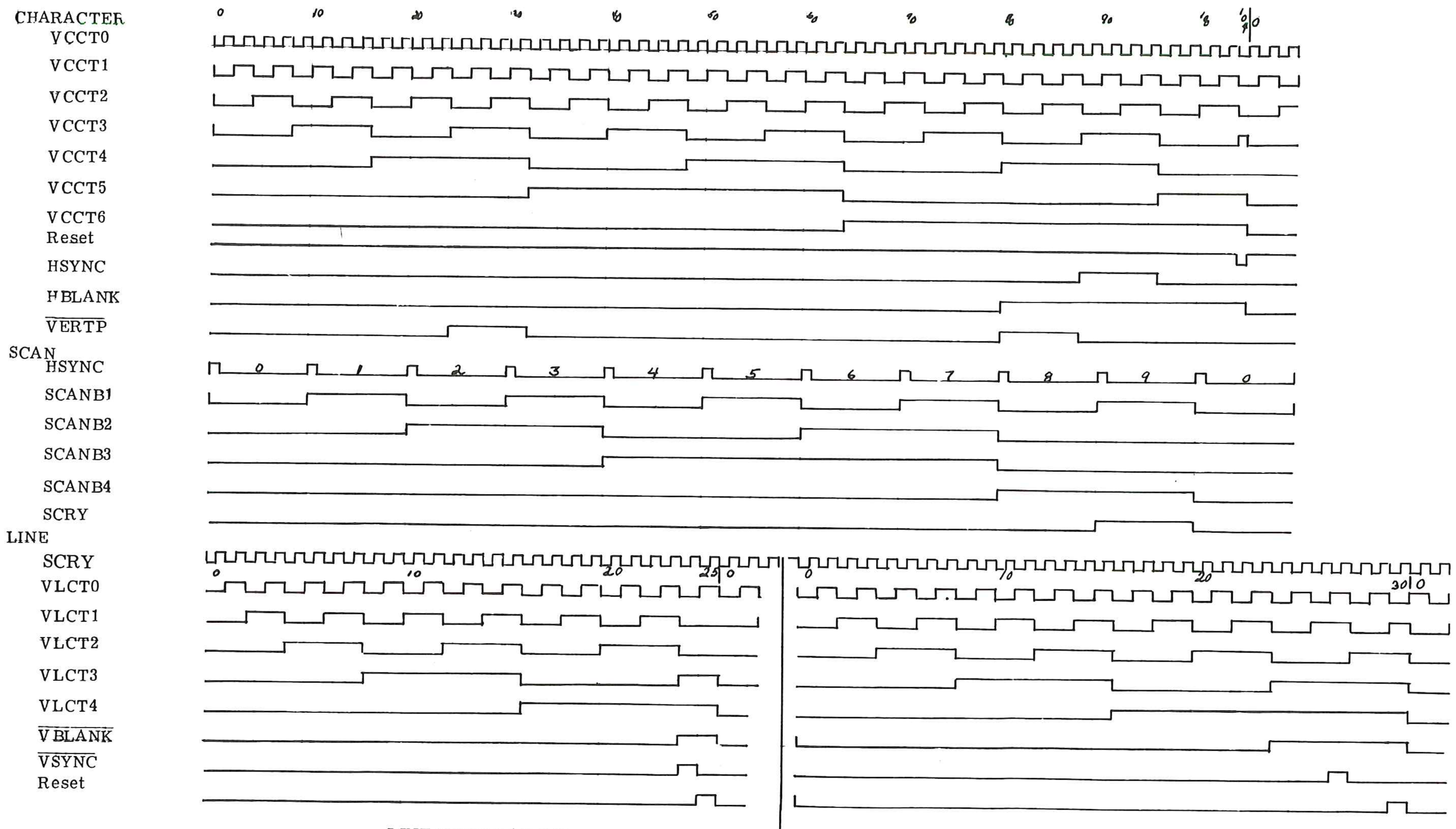
Note:
(#) denotes character or line count.

DISPLAY VIDEO TIMING GENERATOR

VIDEO TIMING AND CHARACTER GENERATOR
001-000942, Sheet 1

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

VIDEO TIMING

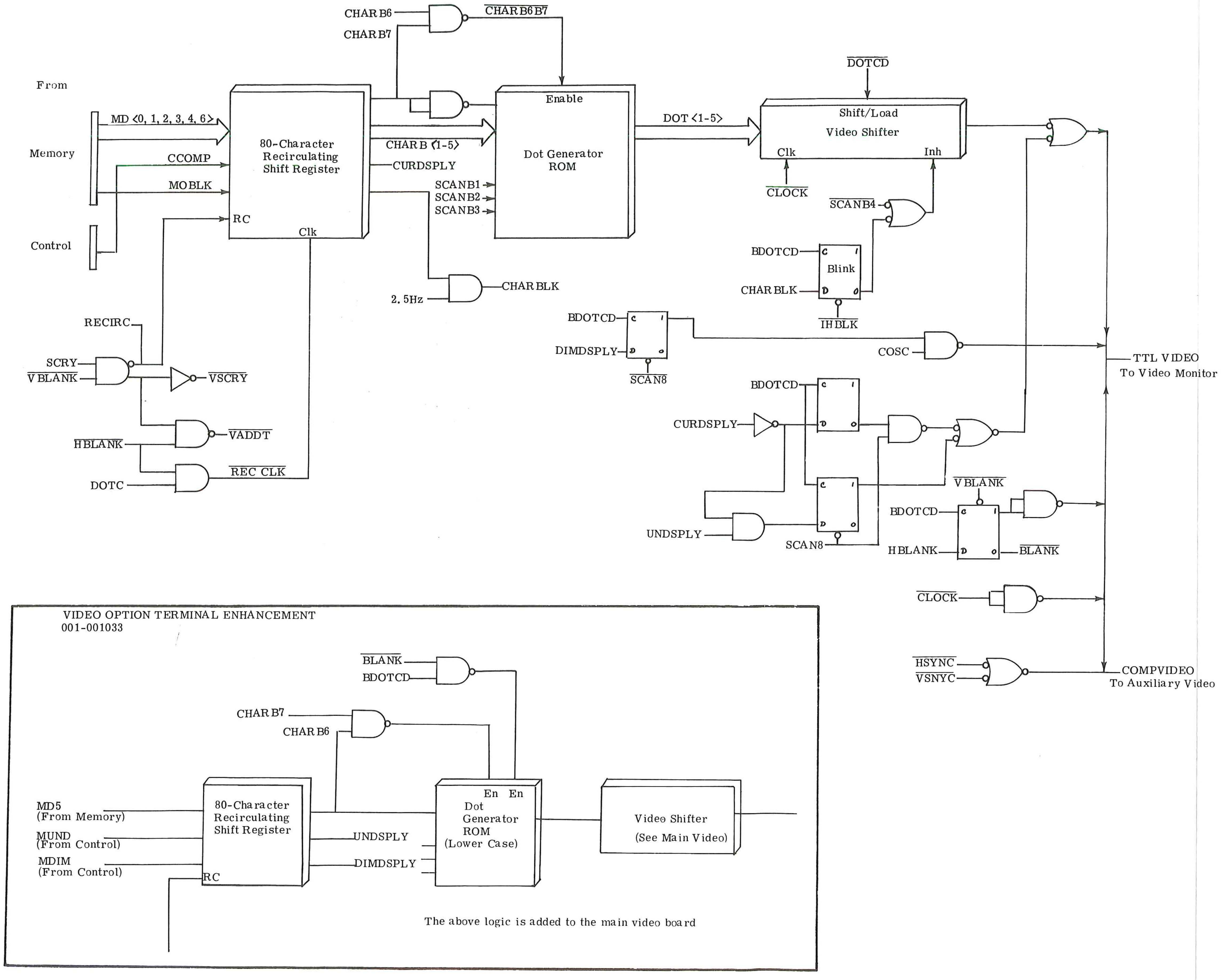


LINE TIMING AT 60Hz

LINE TIMING AT 50Hz

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

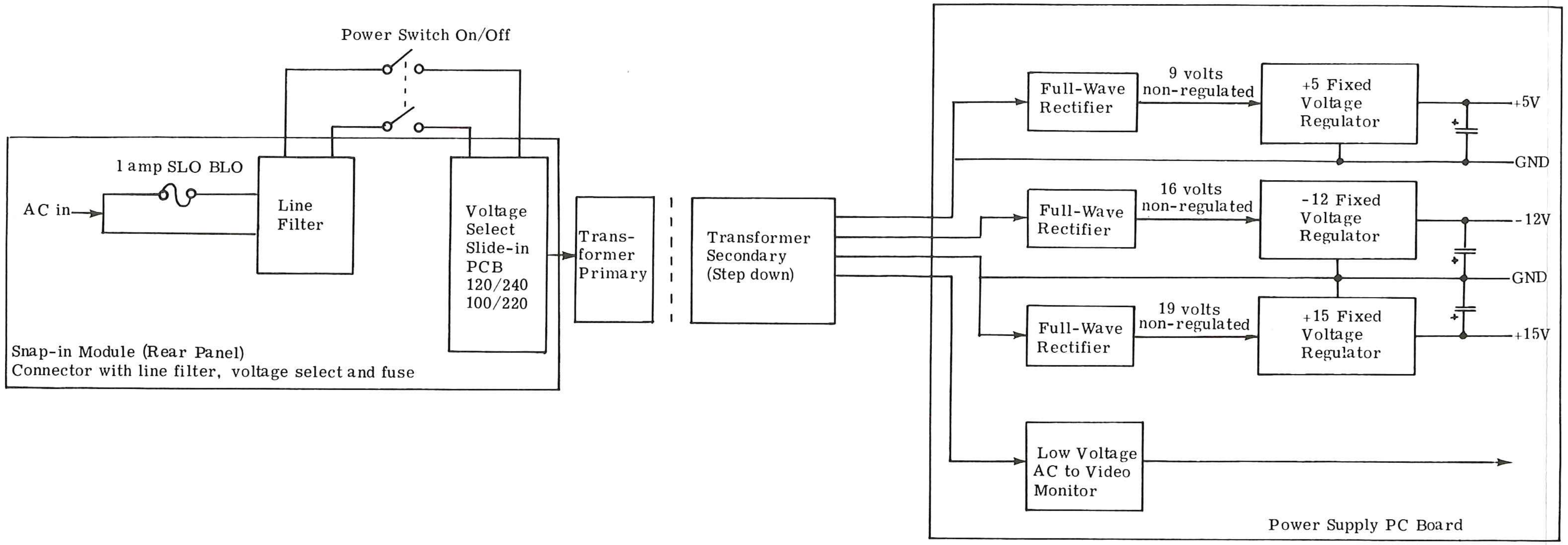
VIDEO CHARACTER GENERATOR
001-000942, Sheet 2



VIDEO OPTION TERMINAL ENHANCEMENT
001-001033

The above logic is added to the main video board

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

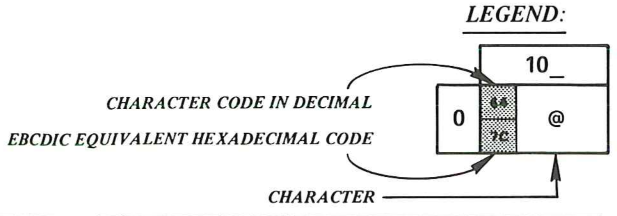

Power Switch On/Off
1 amp SLO BLO
AC in
Line Filter
Voltage Select Slide-in PCB 120/240 100/220
Snap-in Module (Rear Panel)
Connector with line filter, voltage select and fuse
Trans-former Primary
Transformer Secondary (Step down)
Full-Wave Rectifier
9 volts non-regulated
+5 Fixed Voltage Regulator
+5V
GND
Full-Wave Rectifier
16 volts non-regulated
-12 Fixed Voltage Regulator
-12V
GND
Full-Wave Rectifier
19 volts non-regulated
+15 Fixed Voltage Regulator
+15V
Low Voltage AC to Video Monitor
Power Supply PC Board

DISPLAY TERMINAL POWER SUPPLY
001-000948

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

ASCII CHARACTER CODES
WITH DISPLAY TERMINAL, MODELS 6052/6053 CONTROL FUNCTIONS

LEGEND:



↥ *means* CONTROL

OCTAL	00_		CONTROL FUNCTION	01_		CONTROL FUNCTION	02_		CONTROL FUNCTION	03_		CONTROL FUNCTION	04_		05_	
0	0 00	NUL	NULL	8 16	BS *(BACK-SPACE)*	HOME	16 10	DLE ↥P	WRITE CURSOR HEADER	24 18	CAN ↥X	CURSOR RIGHT	32 40	SPACE	40 4D	(
1	1 01	SOH ↥A	PRINT FORM	9 05	HT *(TAB)*	HORIZONTAL TAB	17 11	DC1 ↥Q	PRINT PAGE	25 19	EM ↥Y	CURSOR LEFT	33 5A	!	41 5D	)
2	2 02	STX ↥B	START OF TEXT	10 15	NL *(NEW LINE)*	NEW LINE	18 12	DC2 ↥R	ROLL ON	26 3F	SUB ↥Z	CURSOR DOWN	34 7F	" *(QUOTE)*	42 5C	*
3	3 03	ETX ↥C	ENABLE BLINK	11 0B	VT *(VERT. TAB)*	ERASE LINE	19 13	DC3 ↥S	ROLL OFF	27 27	ESC *(ESCAPE)*	ESCAPE	35 7B	#	43 4E	+
4	4 37	EOT ↥D	INHIBIT BLINK	12 0C	FF *(FORM FEED)*	ERASE PAGE	20 3C	DC4 ↥T	UNDERSCORE ON	28 1C	FS ↥\	DIM ON	36 5B	$	44 6B	, *(COMMA)*
5	5 2D	ENQ ↥E	CURSOR ADDRESS READ	13 0D	RT *(RETURN)*	RETURN	21 3D	NAK ↥U	UNDERSCORE OFF	29 1D	CS ↥]	DIM OFF	37 6C	%	45 60	–
6	6 2E	ACK ↥F	PRINT DONE	14 0E	SO ↥N	BLINK ON	22 32	SYN ↥V	SYNCHRONOUS IDLE	30 1E	RS ↥↑	FUNCTION KEY HEADER	38 50	&	46 4B	. *(PERIOD)*
7	7 2F	BEL ↥G	BELL	15 0F	SI ↥O	BLINK OFF	23 26	ETB ↥W	CURSOR UP	31 1F	US ↥←	READ CURSOR HEADER	39 7D	' *(APOS)*	47 61	/

OCTAL	06_		07_		10_		11_		12_		13_		14_		15_		16_		17_	
0	48 F0	0	56 F8	8	64 7C	@	72 C8	H	80 D7	P	88 E7	X	96 79	` *(GRAVE)*	104 88	h	112 97	p	120 A7	x
1	49 F1	1	57 F9	9	65 C1	A	73 C9	I	81 D8	Q	89 E8	Y	97 81	a	105 89	i	113 98	q	121 A8	y
2	50 F2	2	58 7A	:	66 C2	B	74 D1	J	82 D9	R	90 E9	Z	98 82	b	106 91	j	114 99	r	122 A9	z
3	51 F3	3	59 5E	;	67 C3	C	75 D2	K	83 E2	S	91 AD	[	99 83	c	107 92	k	115 A2	s	123 C0	{
4	52 F4	4	60 4C	<	68 C4	D	76 D3	L	84 E3	T	92 E0	\	100 84	d	108 93	l	116 A3	t	124 4F	¦
5	53 F5	5	61 7E	=	69 C5	E	77 D4	M	85 E4	U	93 BD	]	101 85	e	109 94	m	117 A4	u	125 D0	}
6	54 F6	6	62 6E	>	70 C6	F	78 D5	N	86 E5	V	94 5F	↑ or ∧	102 86	f	110 95	n	118 A5	v	126 A1	~ *(TILDE)*
7	55 F7	7	63 6F	?	71 C7	G	79 D6	O	87 E6	W	95 6D	← or _	103 87	g	111 96	o	119 A6	w̄	127 07	DEL *(RUBOUT)*

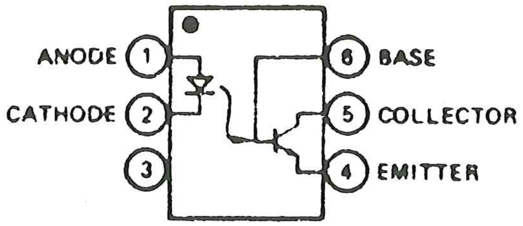
CHARACTER CODE IN OCTAL AT TOP AND LEFT OF CHARTS.

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC's prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

100-000253

Phototransistor Opto-Isolator

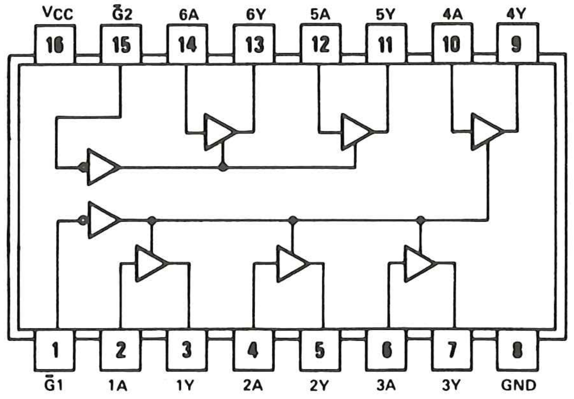
PIN CONFIGURATION



100-000417

Hex Bus Driver With 3-State Outputs

(TOP VIEW)



FUNCTION TABLE
(EACH DRIVER)

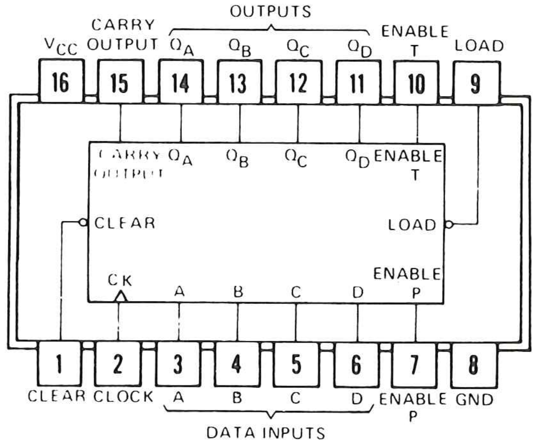
INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Z
L	H	H
L	L	L

H = high level, L = low level,
X = irrelevant, Z = high-impedance

100-000418

Synchronous 4-Bit Counter

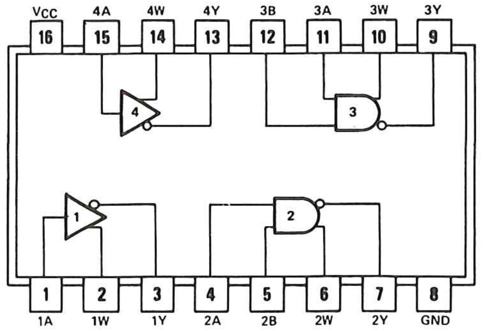
Pin Configuration



NOTE: THE 100-000418 IS A LOW-POWER SCHOTTKY DEVICE.

100-000419

Quad Complementary-Output Elements



positive logic:

ELEMENTS 1 AND 4	ELEMENTS 2 AND 3
Y = $\bar{A}$	Y = $\overline{AB}$
W = A	W = AB

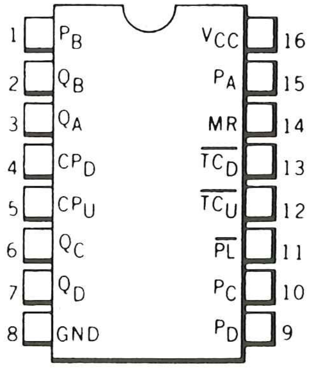
*COMPONENTS NOT FOUND IN DGC COMPONENTS GUIDE 015-000028-03.

DGC PROPRIETARY - This manual contains proprietary information of Data General Corporation (DGC) revealed for the limited purpose only to service DGC equipment on the express condition that the information herein shall not be disclosed to others, and shall not be reproduced in whole or in part, or used in whole or in part as the basis for manufacture or sale of items, without written permission.

100-000467

Up/Down Binary Counters

Pin Configuration



Mode Selection

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

Notes:

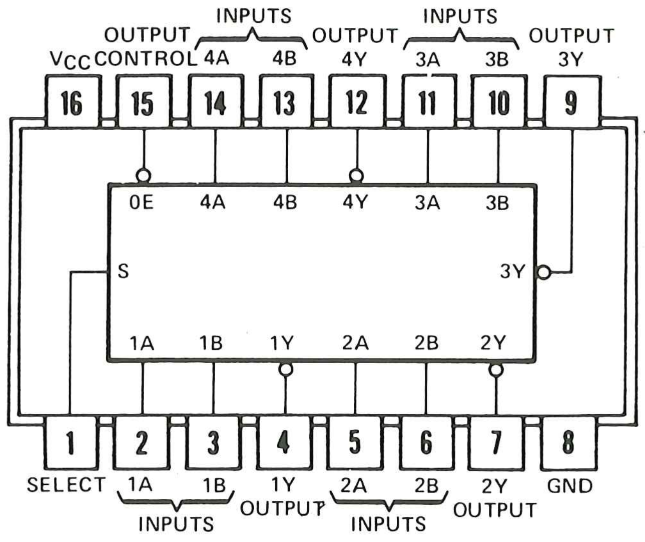
H = High voltage level
L = Low voltage level
X = Don't care condition
CP = Clock pulse.

NOTE: THE 100-000467 IS A LOW-POWER SCHOTTKY DEVICE.

100-000475

Quadruple 2-Line-To-1-Line Data Selectors/Multiplexers

Pin Configuration



V_{CC} = Pin 16
Gnd = Pin 8

Function Table

Inputs			Output
Output Control	Select	A B	Y
H	X	X X	Z
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

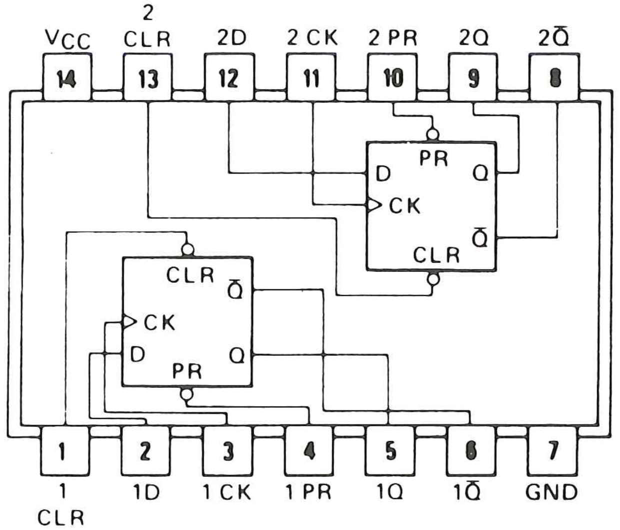
H = high level, L = low level, X = irrelevant,
Z = high impedance (off).

NOTE: THE 100-000475 IS A LOW-POWER SCHOTTKY DEVICE.

100-000476

Dual D-Type Positive-Edge-Triggered Flip-Flops With Preset and Clear

Pin Configuration



Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Function Table

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

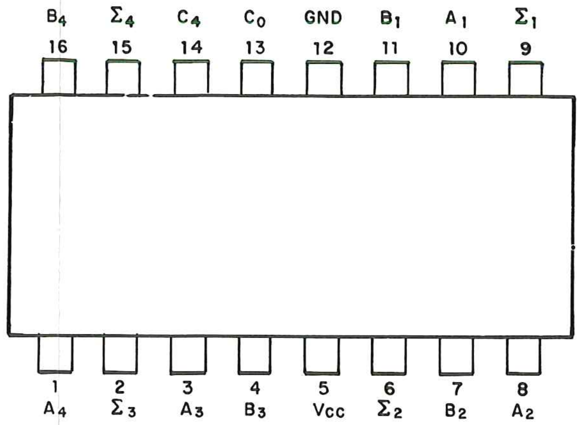
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable: that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE: THE 100-000476 IS A LOW-POWER SCHOTTKY DEVICE.

100-000477

4-Bit Binary Full Adder (Look Ahead Carry)

Pin Configuration



Truth Table

INPUT				OUTPUT					
				WHEN $C_0 = 0$ / WHEN $C_2 = 0$			WHEN $C_0 = 1$ / WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Note:

Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4 and B_4 are then used to determine outputs Σ_3, Σ_4 and C_4.

NOTE: THE 100-000477 IS A LOW-POWER SCHOTTKY DEVICE.

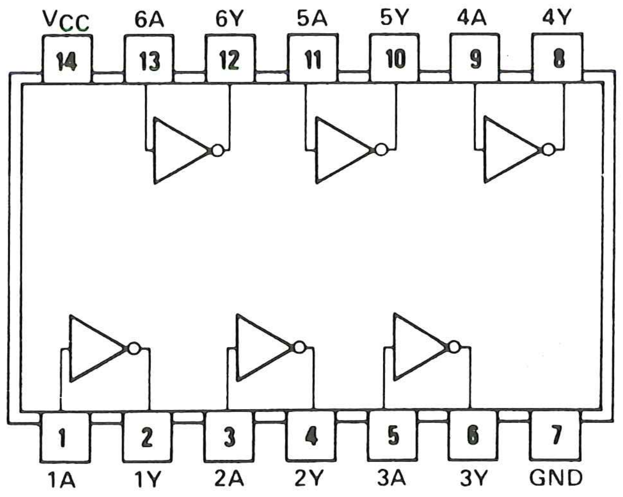
*COMPONENTS NOT FOUND IN DGC COMPONENTS GUIDE 015-000028-03.

DGC PROPRIETARY - This manual contains proprietary information of Data General Corporation (DGC) revealed for the limited purpose only to service DGC equipment on the express condition that the information herein shall not be disclosed to others, and shall not be reproduced in whole or in part, or used in whole or in part as the basis for manufacture or sale of items, without written permission.

100-000576

Hex Inverter

Pin Configuration



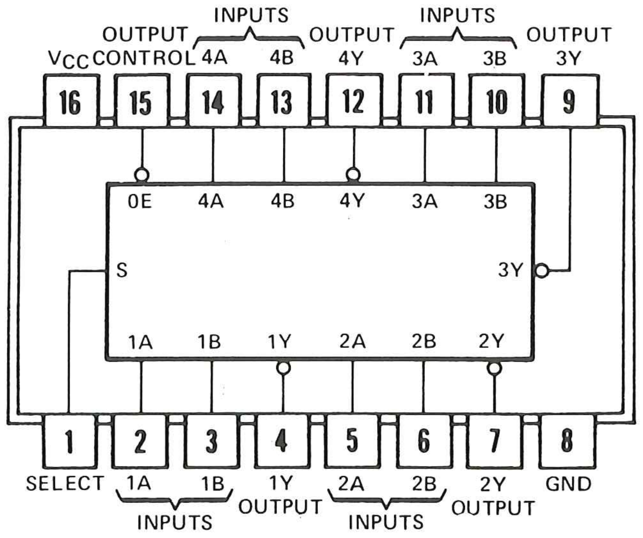
Positive logic: Y = $\overline{A}$

NOTE: THE 100-000576 IS A LOW-POWER SCHOTTKY DEVICE.

100-000577

Quadruple 2-Line-To-1-Line Data Selectors/Multiplexers

Pin Configuration



Function Table

Inputs			Output
Output Control	Select	A B	Y
H	X	X X	Z
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

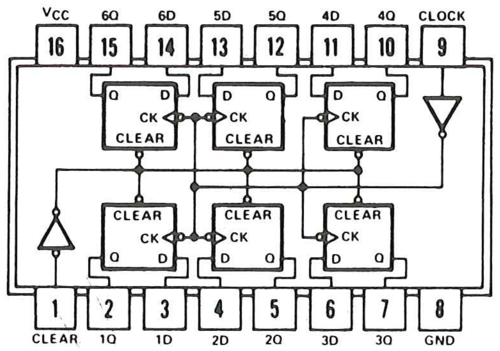
H = high level, L = low level, X = irrelevant,
Z = high impedance (off).

NOTE: THE 100-000577 IS A LOW-POWER SCHOTTKY DEVICE.

100-000578

Hex D-Type Flip-Flops with Clear

Pin Configurations



Function Table
(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Notes:

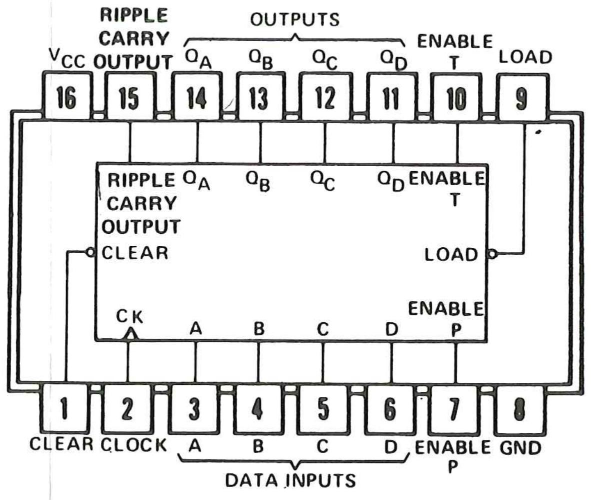
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
* = Type 100000200 and 100000205 only.

NOTE: THE 100-000578 IS A LOW-POWER SCHOTTKY DEVICE.

100-000581

Synchronous 4-Bit Counter

PIN CONFIGURATION



NOTE: THE 100-000581 IS A LOW-POWER SCHOTTKY DEVICE.

DGC PROPRIETARY - This manual contains proprietary information of Data General Corporation (DGC) revealed for the limited purpose only to service DGC equipment on the express condition that the information herein shall not be disclosed to others, and shall not be reproduced in whole or in part, or used in whole or in part as the basis for manufacture or sale of items, without written permission.

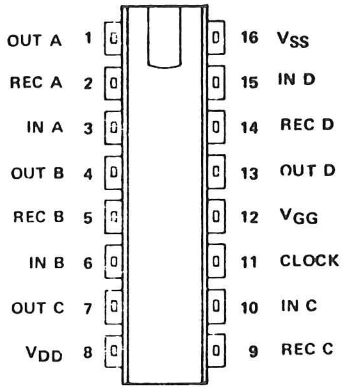
*COMPONENTS NOT FOUND IN DGC COMPONENTS GUIDE 015-000028-03.

100-000585

Quad 80-Bit Dynamic Shift Register

PIN CONFIGURATION

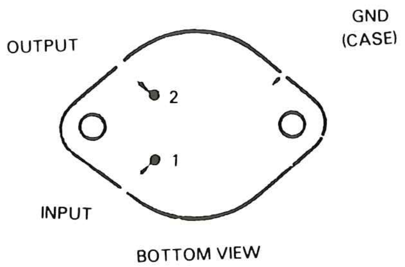
(TOP VIEW)



100-000591

3 Amp - 5 Volt Positive Regulator

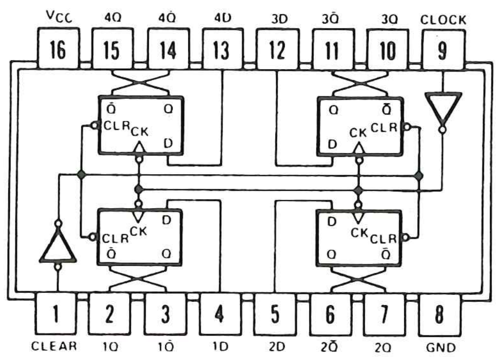
TO-3 (K)



100-000594

Quad D Flip Flop With Clear

PIN CONFIGURATION



Function Table
(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Notes:

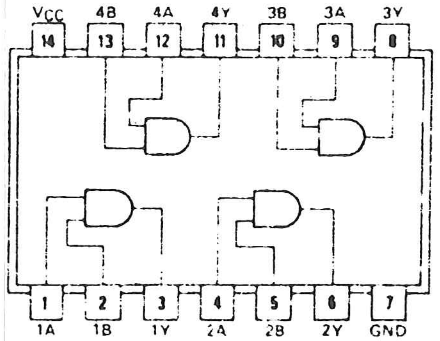
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
* = Type 100000200 and 100000205 only.

NOTE: THE 100-000594 IS A LOW-POWER SCHOTTKY DEVICE.

100-000595

Quad 2-Input Positive-And Gate

PIN CONFIGURATION



NOTE: THE 100-000595 IS A LOW-POWER SCHOTTKY DEVICE.

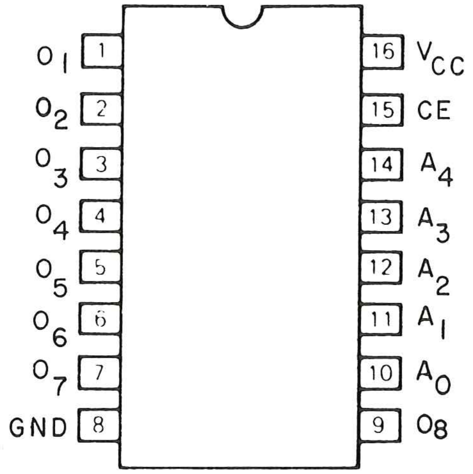
*COMPONENTS NOT FOUND IN DGC COMPONENTS GUIDE 015-000028-03.

DGC PROPRIETARY - This manual contains proprietary information of Data General Corporation (DGC) revealed for the limited purpose only to service DGC equipment on the express condition that the information herein shall not be disclosed to others, and shall not be reproduced in whole or in part, or used in whole or in part as the basis for manufacture or sale of items, without written permission.

100-000786
100-000787
100-000788

256-Bit Bipolar Read Only Memory

Pin Configuration

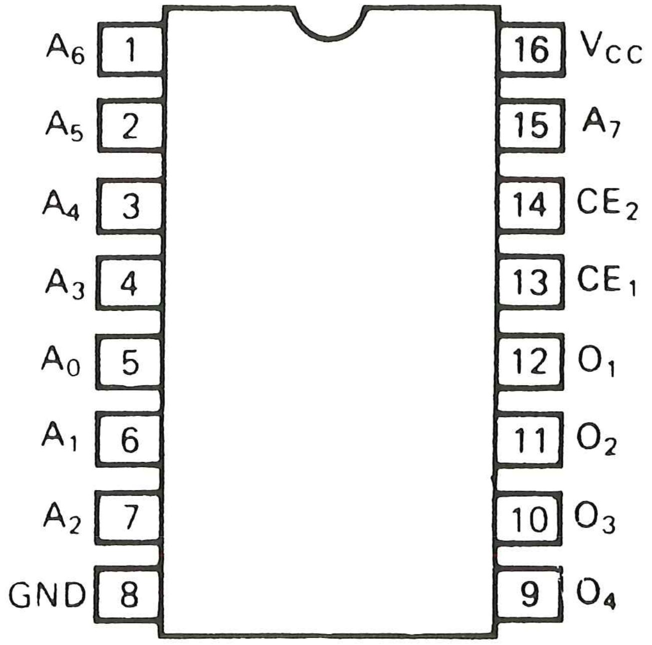


These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

100-000789
100-000790

1024-Bit Programmable Bipolar Read Only Memory

Pin Configuration



Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

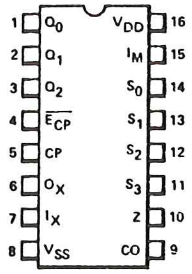
This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

100-000795

Programmable Bit Rate Generator

PIN CONFIGURATION



PIN NAMES

CP	External Clocl Input
$\overline{E_{CP}}$	External Clock Enable Input (Active LOW)
I_X	Crystal Input
I_M	Multiplexed Input
S_0-S_3	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
Q_0-Q_2	Scan Counter Outputs
Z	Bit Rate Output

CLOCK MODES AND INITIALIZATION

I_X	$\overline{E_{CP}}$	CP	OPERATION
⎍⎍⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍	·Reset During First CP = HIGH Time

Note : Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576 MHz.

H = HIGH Level
L = LOW Level
X = Don't Care
⎍ = 1st HIGH Level Clock Pulse After $\overline{E_{CP}}$ Goes LOW
⎍⎍⎍⎍ Clock Pulses

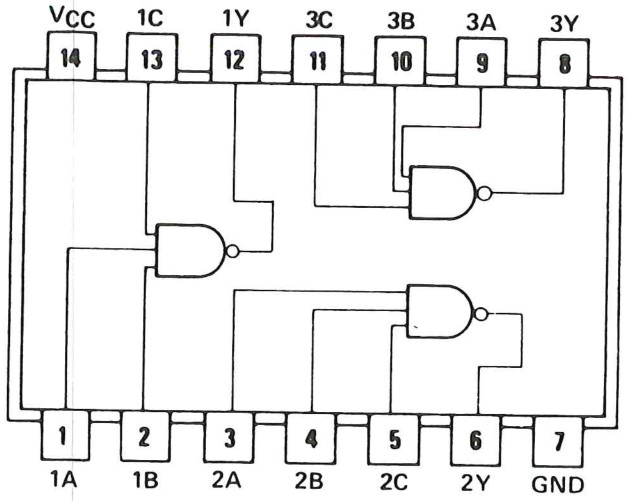
TRUTH TABLE FOR RATE SELECT INPUTS

S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

100-000797

Triple 3-Input Positive-NAND Gate

Pin Configuration



Positive logic: $Y = \overline{ABC}$

NOTE: THE 100-000797 IS A LOW-POWER SCHOTTKY DEVICE.

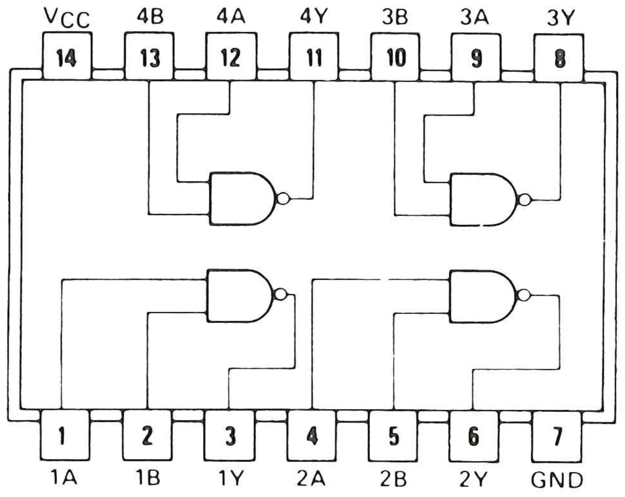
*COMPONENTS NOT FOUND IN DGC COMPONENTS GUIDE 015-000028-03.

DGC PROPRIETARY - This manual contains proprietary information of Data General Corporation (DGC) revealed for the limited purpose only to service DGC equipment on the express condition that the information herein shall not be disclosed to others, and shall not be reproduced in whole or in part, or used in whole or in part as the basis for manufacture or sale of items, without written permission.

100-000799

Quadruple 2-Input Positive-NAND Gate

Pin Configuration



Positive logic: Y = $\overline{AB}$

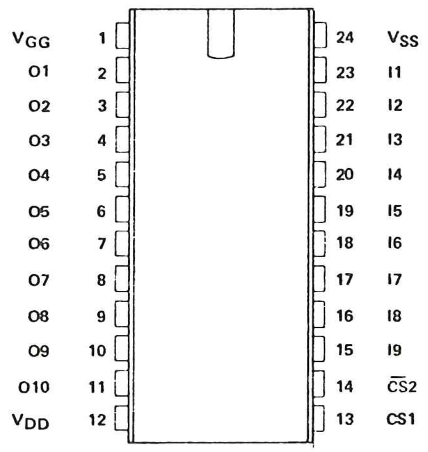
NOTE: THE 100-000799 IS A LOW-POWER SCHOTTKY DEVICE.

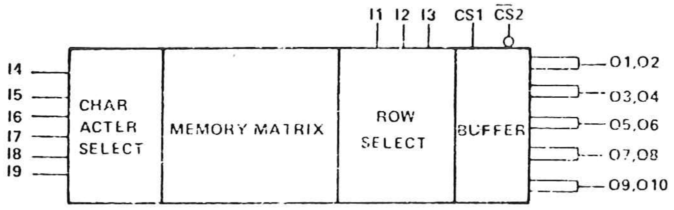
100-000905

64 X 5 X 7 Static USASCII Character Generator

PIN CONFIGURATION

(TOP VIEW)





DGC PROPRIETARY - This manual contains proprietary information of Data General Corporation (DGC) revealed for the limited purpose only to service DGC equipment on the express condition that the information herein shall not be disclosed to others, and shall not be reproduced in whole or in part, or used in whole or in part as the basis for manufacture or sale of items, without written permission.

*COMPONENTS NOT FOUND IN DGC COMPONENTS GUIDE 015-000028-03.

APPENDIX A
PREFIX CODE TABLE

PREFIX CODES	STANDARD TITLING
002	MECH PT (MECHANICAL PART)
005	ASSY (ASSEMBLY B/M PARTS LIST) ASSY DOC PKG (SHIPPED DOCUMENTS)
007	KEY (TOP ASSEMBLY B/M)
008	WL (WIRE LIST FOR CABLES, TEST PLUGS AND INTERCONNECTION WIRING)
010	CONF (CONFIGURATION DRAWING)
011	TEST EQPT (TEST EQUIPMENT)
015	TM (TECHNICAL MANUAL)
016	IPL (ILLUSTRATED PARTS LIST)
029	WIRE PT (WIRE PART)
036	ECO KIT
037	PKG (PACKAGING)
042	TECHNICAL UPDATES
043	FIELD ENGINEERING PUBLICATIONS
044	SHIPPING PACKAGING
100	IC (INTEGRATED CIRCUIT)
101	XISTOR (TRANSISTORS), DIODES
102	RES (RESISTORS)
103	CAP (CAPACITORS)
104	XFMR (TRANSFORMER)
105	CORE FERRITE
106	HDW (HARDWARE)

PREFIX CODES	STANDARD TITLING
108	PUR TEST SPEC (TEST SPEC, PURCHASED PARTS)
109	WIRE, CABLE, TUBING, SLEEVING
110	SWITCH, RELAY
111	HSG (HOUSING), CONN (CONNECTOR), TERM (TERMINAL)
112	CABINET
113	FUSE, FUHLR (FUSE HOLDER)
113	CIR BKR (CIRCUIT BREAKER)
114	INDICATOR, BULB
115	FAN, MOTOR, BLOWER
116	CM (CIRCUIT MODULES)
117	SPEC TOOLS
118	PUR ASSY (PURCHASED ASSEMBLY)
118	PUR PRPHL (PURCHASED PERIPHERALS)
119	MISC PT (MISCELLANEOUS PART)
120	ADHVE (ADHESIVE), TAPE
120	CHEM (CHEMICALS)
121	CRYSTAL
123	STD PT (STANDARD PART)
124	SOLENOIDS
126	METAL STOCK
128	TOOL
129	SHPG MAT (SHIPPING MATERIAL)

This page intentionally left blank.

CUT ALONG DOTTED LINE

READERS COMMENT FORM

DOCUMENT TITLE: ....

Your comments, accompanied by answers to the following questions, help us improve the quality and usefulness of our publications. If your answer to a question is "no" or requires qualification, please explain.

How did you use this publication?

( ) As an introduction to the subject.
( ) As an aid for advanced knowledge.
( ) For information about operating procedures.
( ) To instruct in a class.
( ) As a student in a class.
( ) As a reference manual.
( ) Other..

Did you find the material:

- Useful.............................YES ( ) NO ( )
- Complete.........................YES ( ) NO ( )
- Accurate.........................YES ( ) NO ( )
- Well organized...............YES ( ) NO ( )
- Well written....................YES ( ) NO ( )
- Well illustrated...............YES ( ) NO ( )
- Well indexed...................YES ( ) NO ( )
- Easy to read...................YES ( ) NO ( )
- Easy to understand.......YES ( ) NO ( )

We would appreciate any other comments; please label each comment as an addition, deletion, change, or error and reference page numbers where applicable.

COMMENTS

PAGE	COL	PARA	LINE	FROM	TO

From:

NAME.. TITLE.................................
FIRM... DIV. ....
ADDRESS...
CITY.. STATE.............. ZIP..........
TELEPHONE............................. DATE.................................

Data General Corporation

ENGINEERING PUBLICATIONS
COMMENT FORM
DG-00935

FOLD DOWN FIRST FOLD DOWN

FIRST CLASS
PERMIT NO. 26
SOUTHBORO
MASS. 01772

NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

BUSINESS REPLY MAIL

Postage will be paid by:

DataGeneral
Southboro, Massachusetts 01772

ATTENTION: Engineering Publications

FOLD UP SECOND FOLD UP

STAPLE

DataGeneral

users group

Installation Membership Form

Name ______________________ Position ______________________ Date ____________

Company, Organization or School ____

Address ______________________ City ______________________ State ________ Zip ____________

Telephone: Area Code ____________ No. ______________________ Ext. ______________________

1. Account Category

☐ OEM
☐ End User
☐ System House
☐ Government

2. Hardware

	Qty. Installed	Qty. On Order
M/600		
C/350, C/330, C/300		
S/250, S/230, S/200		
S/130		
AP/130		
CS Series		
N3/D		
Other NOVA		
microNOVA		
Other ____________		
(Specify) ____________		
____________		

3. Software

☐ AOS
☐ DOS
☐ SOS
☐ RDOS
☐ RTOS
☐ Other

Specify ______________________

____

4. Languages

☐ Algol
☐ DG/L
☐ Cobol
☐ ECLIPSE Cobol
☐ Business BASIC
☐ BASIC
☐ Assembler
☐ Interactive
☐ Fortran
☐ RPG II
☐ PL/1
☐ Other

Specify ______________________

____

5. Mode of Operation

☐ Batch (Central)
☐ Batch (Via RJE)
☐ On-Line Interactive

6. Communications

☐ RSTCP
☐ HASP
☐ RJE80
☐ SAM
☐ CAM
☐ 4025
☐ Other

Specify ______________________

____

7. Application Description

○ ______________________

____

____

____

____

____

8. Purchase

From whom was your machine(s) purchased?

☐ **Data General Corp.**
☐ Other
Specify ______________________

____

9. Users Group

Are you interested in joining a special interest or regional Data General Users Group?

○ ______________________

____

DataGeneral

Data General Corporation, Westboro, Massachusetts 01581, (617) 366-8911

FOLD FOLD

STAPLE STAPLE

FOLD FOLD

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 26 SOUTHBORO, MA. 01772

Postage will be paid by addressee:

DataGeneral

ATTN: Users Group Coordinator

Southboro, Massachusetts 01772